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Kirtipur, Kathmandu

**ANALYTICAL EVALUATION OF ROUND ROBIN ALGORITHM  
TO  
FIND THE OPTIMAL QUANTUM SIZE**

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**To My Parents**

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# Abstract

There are a number of scheduling algorithms used in computer systems today. They all have their own characteristics. Thus selection of the particular scheduling algorithm depends upon the need of the system. One of the most widely used scheduling algorithms in multiprogramming operating system is round robin. Primitive round robin scheduling algorithm is simply first-come first-served with preemption included. But, now a days, several variations exist for round robin scheduling algorithm.

In this dissertation, as the title “An analytical evaluation of round robin scheduling algorithm to find the optimal quantum size” suggests, I am going to analyze the round robin scheduling algorithm. There exists different performance criteria to find the optimality of the quantum size but, here, I chose three of them, namely, processor utilization, turnaround time, and waiting time of the processes.

To analyze the round robin algorithm, I simply implemented a simulation of an operating system which we call here a multiprogramming operating system [1]. Different programs are designed for the analysis purpose which we call here the workload. With the help of simulator and the workload, I analyzed the different performance criteria for different quantum sizes and, came to the conclusion for this dissertation work.

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# Abbreviations

<b>CPU</b>	Central Processing Unit
<b>SI</b>	Supervisor Interrupt
<b>PI</b>	Program Interrupt
<b>TI</b>	Timer Interrupt
<b>IOI</b>	Input Output Interrupt
<b>RQ</b>	Ready Queue
<b>TQ</b>	Terminate Queue
<b>LQ</b>	Load Queue
<b>SQ</b>	Swap Queue
<b>IOQ</b>	Input Output Queue
<b>EB</b>	Empty Buffer
<b>EBQ</b>	Empty Buffer Queue
<b>IFB</b>	Input Full Buffer
<b>IFBQ</b>	Input Full Buffer Queue
<b>OFB</b>	Output Full Buffer
<b>OFBQ</b>	Output Full Buffer Queue
<b>IR</b>	Instruction Register
<b>IC</b>	Instruction Counter
<b>C</b>	Boolean toggle

<b>PTR</b>	Page Table Resister
<b>PCB</b>	Process Control Block
<b>CHST</b>	Channel Status
<b>LLC</b>	Line Limit Counter
<b>TLL</b>	Total Line Limit
<b>TTC</b>	Total Time Counter
<b>TTL</b>	Total Time Limit
<b>TSC</b>	Time Slice Counter
<b>TS</b>	Time Slice