Tribhuvan University

Institute of Science and Technology

Quantitative Evaluation of Buffer Replacement Algorithms for Flash Memory Based Systems

Dissertation

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in partial fulfillment of the requirements for the award of degree of

Master of Science in

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By

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Supervisor

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January, 2014

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Student's Declaration

I hereby declare that I am the only author of this work and that no sources other than the listed here have been used in this work.

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Date: 22 January, 2014

Supervisor's Recommendation

I hereby recommend that this dissertation prepared under my supervision by Mr. **Bikram Bahadur Rawat** entitled **"Quantitative Evaluation of Buffer Replacement Algorithms for Flash Memory Based Systems"** in partial fulfillment of the requirements for the award of degree of M.Sc. in Computer Science and Information Technology be processed for the evaluation.

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LETTER OF APPROVAL

We certify that we have read this dissertation and in our opinion it is satisfactory in the scope and quality as a dissertation in the partial fulfillment for the requirement of Masters Degree in Computer Science and Information Technology.

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Abstract

The ever increasing requirement for high performance and high capacity memories of emerging handheld devices or applications has led to the widespread adoption of DRAM and NAND type flash memories. Thus, the buffering policy for flash based systems has to improve the overall performance.

Hence, the use of flash memory requires new buffer replacement policies considering not only buffer hit and miss rates but also the number of read , write and erase operations. Most of the traditional buffer replacement algorithms focued on the hit ratio improvement alone, but not the number of write counts caused by dirty pages to be propagated to the flash memory, which is the main factor to be considered in flash memory based systems.

The dissertation is mainly focused initially to determine the optimal window size for Clean First LRU algorithm and then to evaluate the performance of LRU, CFLRU and ADLRU buffer replacement algorithms. Finally, the comaparative study based on quantitative analysis of those algorithms is performed based on the hit/miss rates and the number write counts. The evaluation is conducted in a simulation environment using three kinds of synthetic traces : random, readmost, and writemost. The dissertation finally concluded that the ADLRU is superior to LRU and CFLRU in most of the cases. Hence, for flash based systems, the ADLRU buffer replacement algorithm is the best option due to its high hit rates and at the same time low write counts.

Keywords:- Flash Memory, replacement policy, buffer management, LRU page replacement algorithm, Clean First LRU (CFLRU) buffer replacement algorithm, Adaptive LRU (ADLRU) buffer replacement algorithm, Page faults, Cold LRU, Hot LRU, write counts, hit rate, miss rate.

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List of Abbreviations

ADLRU	–	Adaptive Least Recently Used
ARC	-	Adaptive Replacement Cache
CASA	–	Cost Aware Self Adaptive
CFDC	–	Clean First Dirty Clustered
CFLRU	–	Clean First Least Recently Used
CMOS	–	Complementary Metal Oxide Semiconductor
CPU	-	Central Processing Unit
DLL	–	Doubly Linked List
DRAM	-	Dynamic RAM
EEPROM	–	Electrically Erasable Programmable Read Only Memory
HPC	–	Handheld Personal Computer
HR	-	Hit Rate
IDE	–	Integrated Development Environment
I/O	–	Input / Output
JIT	–	Just In Time
JVM	–	Java Virtual Machine
LFU	-	Least Frequently Used
LIRS	-	Low Inter-reference Recency Set
LRFU	-	Least Recently Frequently Used
LRU	-	Least Recently Used
MLC	–	Multi Level Cell
MR	-	Miss Rate
MRU	-	Most Recently Used
NAND	–	NOT AND
NDP	-	Number of Distinct Pages
NPF	-	Number of Page Fault
NRU	-	Not Recently Used
OS	–	Operating System
PDA	–	Personal Digital Assitant
PMP	–	Portable Media Players
SLC	–	Single Level Cell
XIP	–	eXecute In Place