TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
PULCHOWK CAMPUS

A
FINAL YEAR PROJECT REPORT
ON
DESIGN AND HARDWARE IMPLEMENTATION OF MULTILEVEL INVERTER

(Submitted to the Department of Electrical Engineering as partial fulfillment of the requirement for the Bachelor in Electrical Engineering) **(EE755)**

PROJECT MEMBERS

Bharat Kumar Sah (PUL075BEL009)
Chandan Thakur (PUL075BEL013)
Sagar Goswami (PUL075BEL039)
Ujjwal Kadel (PUL075BEL046)

PROJECT SUPERVISORS

Asst. Prof. Shahabuddin Khan
Asst. Prof. Ganesh Bhandari

April 27, 2023

TRIBHUVAN UNIVERSITY

INSTITUTE OF ENGINEERING

DEPARTMENT OF ELECTRICAL ENGINEERING

The undersigned certifies that they have read and recommended to the Institute of Engineering for acceptance, a project report entitled **"DESIGN AND HARDWARE IMPLEMENTATION OF MULTILEVEL INVERTER"** submitted by Bharat Kumar Sah, Chandan Thakur, Sagar Goswami and Ujjwal Kadel in the partial fulfillment of the requirements for the Bachelor's Degree in Electrical Engineering.

Project Supervisor

Asst. Prof. Shahabuddin Khan

Department of Electrical Engineering

Pulchowk Campus

Project Supervisor

Asst. Prof. Ganesh Bhandari

Department of Electrical Engineering

Pulchowk Campus

Head of Department

Asst. Prof. Yubraj Adhikari

Department of Electrical Engineering

Pulchowk Campus

External Examiner

Mr. Rajan Dhakal

Director, NEA

DCS, Bagmati Provincial Office

Date of approval: 2023/04/27

COPYRIGHT©

ACKNOWLEDGEMENT

We would like to express our sincere gratitude to everyone who helped us throughout the project completion in one way or another. A very special thanks to our Supervisors Asst. Prof. Shahabuddin Khan and Asst. Prof. Ganesh Bhandari whose tremendous guidance, stimulating suggestions and encouragement helped us in all time of guiding the project towards completion. We also sincerely thank him for the time spent correcting mistakes and providing alternatives whenever necessary.

We would like to express our deep respect to Head of Electrical Engineering Department for their academic and administrative support. Many thanks to all the lecturers and professors of the Department of Electrical Engineering for their invaluable suggestions and support throughout the project. We are thankful to the authors of various research articles that we referred to during the course of the project.

We would like to extend our sincere regards to all the staff members of the Department for their cooperation. Last but not the least, we are extremely grateful to our friends and families who has always supported us in different ways and helped us directly or indirectly in completing the project.

Bharat Kumar Sah

Chandan Thakur

Sagar Goswami

Ujjwal Kadel

ABSTRACT

An inverter is utilized to transform a DC source into an AC source using power electronic components. It can be achieved using two types of inverters, one is two level inverter and another is multilevel inverter (MLI). MLI has been implemented in various applications, such as motor drives, power conditioning devices, renewable energy generation and distribution. PWM inverters can simultaneously control output voltage, frequency and it can reduce the THD content in output waveform.

This project aims in the study of different MLI topologies, primarily focused in the study of Cascaded H bridge (CHB) and Switched Capacitor MLI (SCMLI). Several multilevel topologies have been developed, but as the output voltage level increases, it also increases the number of switches, switching stresses, losses and voltage unbalancing across the capacitors, etc. CHBMLI is more efficient compare to the other topologies of multilevel inverter but not as efficient as Switched Capacitor MLI. SCMLIs are the most widely used because of self-voltage balancing and voltage boosting over conventional ones with reduced number of DC sources.

In this project, simulation of single phase CHB and SC MLI: 5 level, 9 level and 17 level is done and hardware implementation of 3 level and 5 level CHB MLI is done. The simulation involves utilizing Simulink and Proteus to model and analyze different MLIs. By employing appropriate control strategies, the performance and THD of each MLI topology is evaluated. The simulation results provide valuable insights into the feasibility and effectiveness of these MLIs. Furthermore, a hardware implementation of the 3-level and 5-level CHB MLI is conducted. This involves designing the necessary circuitry, selecting suitable power devices, and implementing control algorithms. Standard high voltage components were chosen for MOSFET drivers Through the hardware setup, we aim to validate the simulation results and assess the practical aspects of MLIs such as switching losses, thermal behavior, and real-time performance.

Ultimately, this project contributes to the advancement of MLI technology by presenting comprehensive simulation studies and practical hardware implementations of different MLIs. The findings can guide future researchers in selecting the most suitable MLI topology for specific power conversions considering factors like complexity, THD and cost-effectiveness.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AC	- Alternating Current
CHB	- Cascaded H Bridge
DC	- Direct Current
FMLI	- Flying capacitor Multilevel Inverter
Hz	- Hertz
MLI	- Multilevel Inverter
NMLI	- Neutral Point Clamped Multilevel Inverter
PV	- Photovoltaics
SC	- Switched Capacitor
SMPS	- Switched Mode Power Supply
STATCOM	- Static var Compensator
THD	- Total Harmonic Distortion

CHAPTER ONE
INTRODUCTION

1.1 Background

MLIs have become highly popular in various power applications, thanks to their capability of generating output similar to a sinusoidal waveform by utilizing DC sources & switches. These inverters incorporate capacitors & diodes to enhance their structural flexibility. MLIs find extensive usage in diverse areas such as photovoltaic systems, high-frequency power distribution, traction drives, EVs, STATCOM and more. Their deployment in these domains aims to improve efficiency, power quality & reliability [2].

MLIs are gaining increasing recognition as converters due to their numerous structural advantages, including easy scalability, lower voltage stress (dv/dt), balanced load sharing & efficient energy harvesting. These features make MLIs highly appropriate for numerous renewable energy applications. Switched capacitor MLIs (SCMLIs) are widely adopted among the different types of MLIs due to their ability to boost voltage compared to conventional MLIs while utilizing fewer DC sources. Cascaded MLIs aim to generate a higher number of voltage levels, thus reducing the number of devices required. However, this approach leads to higher blocking voltages and lacks the voltage boosting feature [4].

Hybrid multilevel inverters (MLIs) offer the advantage of reducing the number of semiconductor devices while allowing for an increased no. of voltage levels. This can be achieved by cascading multiple units or incorporating a backend H-bridge. However, a drawback of hybrid MLIs is the occurrence of high blocking voltage when the number of semiconductor elements is increased. When subunits of SCMLIs (switched capacitor MLIs) are cascaded to achieve the required output voltage, using an increased number of capacitors in parallel results in a larger boosting ratio but also leads to high blocking voltage. Consequently, this causes increased conduction losses & switching losses. Nonetheless, SC MLIs are well-suited for high-frequency AC power distribution & photovoltaic applications as they can balance voltage in the switched capacitors without the use of additional sensors & provide boosting of input voltage without the need for extra inductors or transformers [6].

1.2 Problem statement

The neutral-point clamped (NMLI), flying-capacitor MLI (FMLI), and cascaded H-bridge MLI (CMLI) are well-known topologies used in multilevel inverters (MLIs). However, both NMLI and FMLI encounter challenges associated with voltage balancing and the risk of module collapse with switches connected in series. In contrast, CMLI eliminates the need for extra clamping diodes/capacitors. Nonetheless, all these MLIs require a significant number of semiconductor devices to generate higher output level. In case of CMLI, capacitors are utilized to lower the no. of DC inputs and produce various voltage output levels. However, the boosting factor of voltage (the ratio of output voltage to the input voltage) remains at 1, which poses a limitation. This limitation is particularly critical in photovoltaic (PV) systems, where matching the voltage with the grid/load requirements is crucial. To achieve voltage boosting in PV systems, an additional DC-DC booster becomes necessary, introducing complexity and cost to the overall system.

1.3 Objectives

1.3.1 Main Objectives

- ❖ To reduce the THD level acceptable as per the IEEE standards.

1.3.2 Specific Objectives

- To improve the quality of output by reducing the losses.
- To study about different types of MLIs and compare them.
- To reduce the cost of the MLI by using a lesser number of components.
- To operate the circuit under any loading power factor (PF).

1.4 Scope and limitation

The working and output waveform of different types of Multilevel Inverters is observed along with the calculation of total harmonic distortion. The scope multilevel inverter project includes research and development, high power applications, improved power quality and scalable and modular designs.

Multilevel inverter projects can provide opportunities for exploring new concepts, developing innovative solutions, and contributing to the advancement of power electronics

and renewable energy systems. These projects can focus on developing and implementing these systems for various high-power applications, addressing the growing demand for clean energy and efficient power conversion. Multilevel inverter projects can explore advanced modulation techniques, control algorithms, and optimization strategies to enhance the power quality of grid-connected systems, microgrids, and other applications sensitive to harmonic distortion. Multilevel inverters can be designed with a scalable and modular approach, allowing for easy expansion and adaptation to different voltage levels, power levels, and applications.

Limitations includes complexity and costs, system integration challenges, thermal management and control complexity. Multilevel inverter projects can be complex and costly due to the multiple power electronic devices, complex control algorithms, and advanced modulation techniques involved. Integrating multilevel inverters into existing power systems or applications may pose challenges, such as compatibility issues, system interactions, and coordination with other power electronic devices. Multilevel inverters can generate significant heat due to the high voltage levels and switching frequencies involved. Advanced cooling techniques, thermal modeling, and optimization strategies may be required to address the thermal challenges. Control of multilevel inverters can be complex due to the increased number of voltage levels, multiple power electronic devices, and advanced modulation strategies.

1.5 Project outline

i. This project constitutes five chapters including the current chapter. This chapter explains about the basic introduction about different types of MLIs. Also, it covers the statement of the problem, objective of this project, and scopes and limitations.

ii. Chapter two presents a comprehensive literature review, encompassing theoretical studies, articles or publications from IEEE conferences or transactions, and books from prominent publishers. The aim is to gather existing information and previous findings from other researchers in order to establish a solid knowledge base.

iii. Chapter three includes the proposed system and working of the project and the methods and tools that were implemented to attain the objectives of the project. Also, the necessary components and required circuits are described in this chapter.

iv. Chapter four presents the simulation results and hardware output that have been obtained during the implementation of this project. Also, the discussion on the obtained results is performed.

v. Chapter five gives conclusion and recommendation about this project.

CHAPTER TWO
LITERATURE REVIEW

2.1 Review of paper

The concept of the Multi-Level Inverter (MLI) dates back to the 19th century when it was introduced to effectively manage low-level voltages by incorporating a higher number of switches, resulting in minimized output steps. This approach aimed to produce power waveforms of higher quality while reducing voltage stress on the load and addressing electromagnetic compatibility concerns. Recent advancements have proposed new approaches, including topologies utilizing low-switching-frequency high-power devices. However, despite efforts to reduce output voltage distortion, this method still suffers from significant low-order current harmonics. Additionally, the adopted pulse width modulation (PWM) method limits precise control over the output voltage magnitude [9].

Capacitor clamped inverters make use of a flying capacitor to regulate voltage, leveraging its ability to charge and discharge. This enables effective control of both the input source and the output. Compared to diode clamped inverters, capacitor clamped inverters offer enhanced voltage synthesis and greater flexibility. By cascading the two circuits with a minimal number of components, not only is the component count reduced, but it also explores methods to improve the output voltage level by increasing the number of steps [10].

Cascaded multilevel inverters (MLIs) are employed to achieve a larger number of voltage levels while minimizing the required number of devices. However, this approach often leads to high blocking voltage and lacks the voltage boosting feature [2].

The switching capacitor topology allows for voltage boosting to multiple output levels, with capacitors playing a crucial role in this process. The use of an H-bridge enables the generation of stepped output. However, when cascading subunits of the switched capacitor multilevel inverter (SCMLI) to achieve a desired output voltage with an increased number of capacitors in parallel connection, a high boosting ratio is achieved. Unfortunately, this configuration also results in high blocking voltage, leading to increased switching losses and conduction losses [4]. The ability of switched capacitor multilevel inverters (SC MLIs) to balance the voltages of switched capacitors (SCs) without the need for auxiliary sensors, and their

capability for voltage boosting without additional inductors or transformers, make them well-suited for high-frequency AC power distribution & PV applications [6].

2.2 Related theories

2.2.1 Working principle of multilevel inverters

Multilevel inverters are electronic devices used to convert direct current (DC) power into alternating current (AC) power, providing multiple voltage levels. They are extensively used in high-power systems such as motor drives, renewable energy setups, and grid-connected systems. Multilevel inverters operate by combining different levels of DC voltages to synthesize a stepped waveform, resulting in an AC output waveform with lower harmonic distortion compared to traditional two-level inverters.

Typically, a multilevel inverter comprises a series of power semiconductor devices like insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs), along with capacitors. These components are interconnected in a specific configuration to achieve the desired voltage levels. A 3-level neutral point clamped inverter (NPC)'s output voltage can be expressed mathematically as follows:

For the upper arm (positive side) of the inverter:

$V_{ab} = V_{dc} * (2 * ma - 1)$ …… …… (2.1)

For the lower arm (negative side) of the inverter:

$V_{ac} = -V_{dc} * (2 * mb - 1)$ ……(2.2)

Here, V_{ab} represents the output voltage between phase a and phase b, Vac represents the output voltage between phase a and phase c, V_{dc} is the DC input voltage, and ma and mb are the modulation indices for phases b and c, respectively. The modulation indices vary between 0 and 1.

The modulation indices (ma and mb) determine the width of the Pulse Width Modulation (PWM) pulses applied to the upper and lower arms of the inverter. By controlling the switching of the power devices, the desired output voltage levels can be achieved. The modulation indices can be adjusted to vary the output voltage levels and the harmonic content of the output waveform.

2.2.2 Modulation Techniques for MLI

Carrier based Pulse Width Modulation (PWM) techniques are categorized into two primary categories: level-shifted modulation & phase shifted modulation. Both techniques necessitate (m-1) triangular carrier waves for an m-level inverter. It is crucial that all the carrier waves share the same frequency and peak-to-peak magnitude.

2.2.2.1 Phase shifted PWM

Phase shifted carrier modulation is a commonly employed technique in the industry for multi-level H-bridge converters. This modulation scheme provides a notable advantage over level shifted and space vector modulation schemes by evenly distributing losses among the semiconductor devices. However, the conventional implementation of this scheme necessitates a capacitor voltage balancing scheme, which can affect the converter's harmonic performance

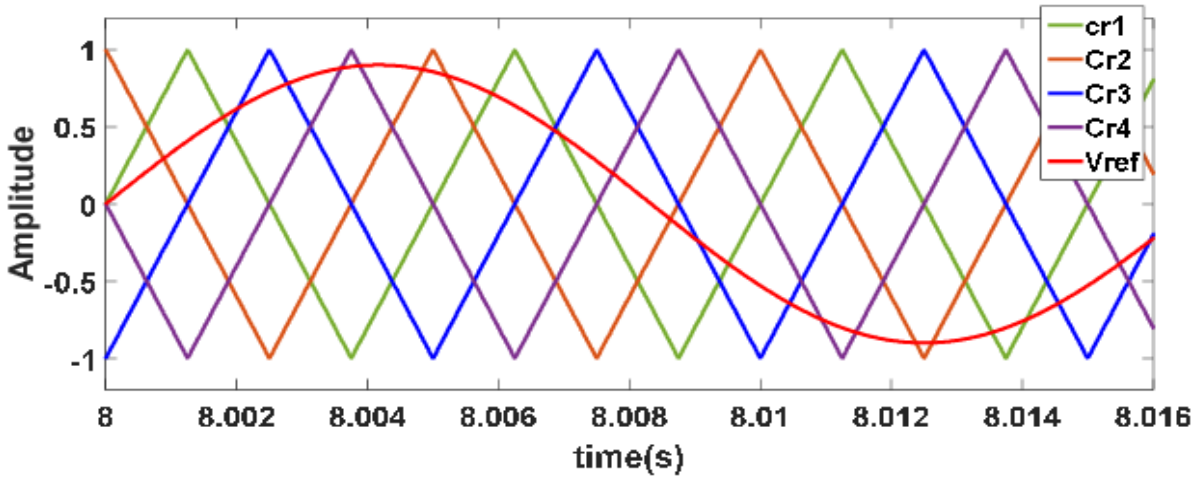


Figure 1: Phase Shifted PWM [5]

2.2.2.2 Phase Disposition PWM

The phase disposition modulation technique, also referred to as level-shifted PWM, entails aligning all triangular carriers in phase and stacking them on top of each other, as depicted in the figure 2. These stacked triangular carriers are subsequently compared with a reference waveform to generate pulses for the switches in the multilevel inverter. This technique is highly regarded for its ability to minimize harmonic distortion in voltage (line to line).

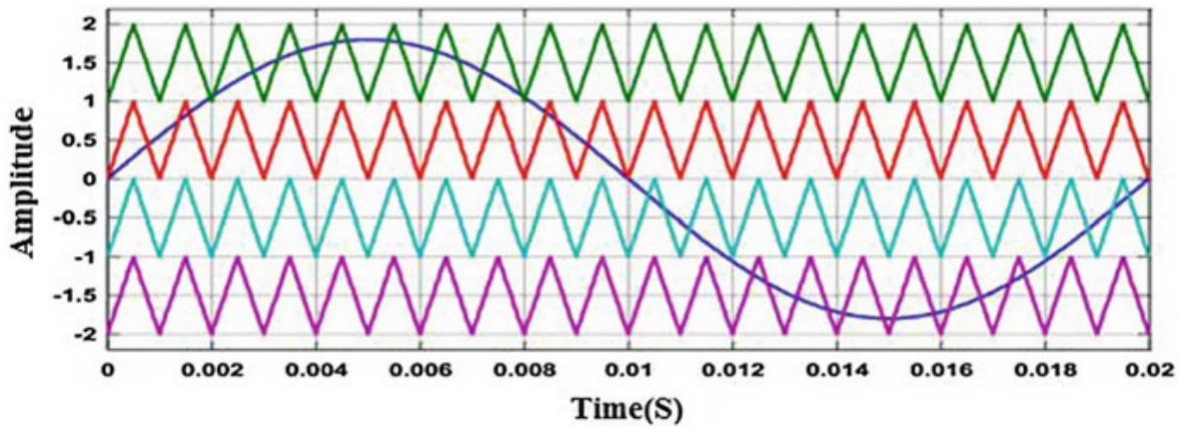


Figure 2: Carrier wave and reference wave for 5-level CHB MLI with PD-PWM [5]

2.2.3 Gate triggering of Power MOSFETs

Gate triggering refers to the process of applying a voltage or current signal to the gate terminal of a power MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) to turn it on or off. Power MOSFETs are widely used in various applications, including power electronics, motor drives, switching power supplies, and other high-voltage and high-current circuits.

There are several methods for gate triggering of power MOSFETs, depending on the specific circuit requirements and the characteristics of the MOSFET being used. Some common gate triggering methods for power MOSFETs include:

1. Direct Gate Drive: In this method, a voltage signal is directly applied to the gate terminal of the MOSFET to turn it on or off. Typically, a gate driver circuit is used to provide a controlled and sufficient voltage level to the gate of the MOSFET to ensure reliable switching. The gate driver circuit may include level shifters, voltage regulators, and other components to protect the MOSFET from excessive voltage or current stresses.

2. Resistive Gate Drive: In this method, a resistor is used to drive the gate of the MOSFET. The resistor limits the current flowing into the gate terminal, which helps to prevent excessive current and voltage stresses on the MOSFET during switching. However, resistive gate drive can be slower compared to other methods due to the RC time constant of the resistor-capacitor (RC) network formed by the gate capacitance of the MOSFET and the gate resistor.

3. Opto-Isolated Gate Drive: In this method, an opto-isolator, such as an optocoupler, is used to transfer the gate drive signal to the MOSFET. The opto-isolator provides isolation between the input and output circuits, similar to the transformer-coupled gate drive method. It requires an external power supply to drive the opto-isolator and may have limitations in terms of speed and power capability.

The specific gate triggering method used for power MOSFETs depends on the requirements of the application, such as switching speed, voltage level, current level, and isolation requirements. Proper gate triggering is important to ensure reliable and efficient operation of power MOSFETs in various circuit applications. It is recommended to consult the MOSFET datasheet and application notes for the specific MOSFET being used to determine the appropriate gate triggering method and associated circuitry. Additionally, proper gate driver design, including considerations such as gate voltage levels, gate capacitance, gate resistance, and transient protection, should be taken into account to ensure safe and reliable operation of power MOSFETs.

CHAPTER THREE
METHODOLOGY

3.1 Operating modes/Working of cascaded 5-level H bridge MLI

Mode1: +2Vdc: In this mode, switches SW1, SW2, SW5 and SW6 are ON and all the other switches SW3, SW4, SW7 and SW8 are OFF.

Mode2: +Vdc: In this mode, switches SW1, SW2, SW8 and SW6 are ON and all the other switches SW3, SW4, SW7 and SW5 are OFF.

Mode3: 0: The lower-leg switches are triggered; thus no flow of current in the power circuit.

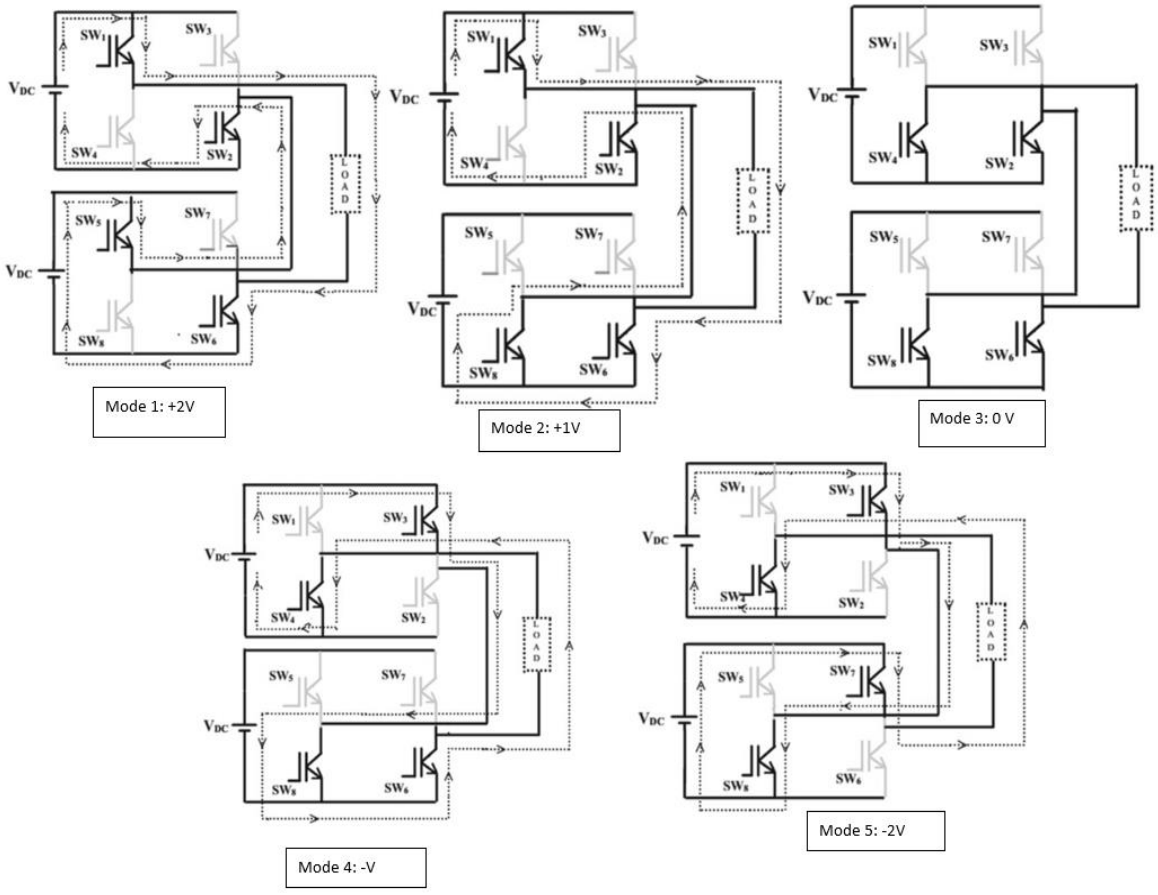


Figure 3: Modes of operation of 5 level CHB MLI

Mode 4: −Vdc: In this mode, switches SW3, SW4, SW8 and SW6 are ON and all the other switches SW1, SW2, SW7 and SW5 are OFF. The current flow and load current are opposite.

Mode 5: -2Vdc: In this mode, switches SW3, SW4, SW8 and SW7 are ON and all the other switches SW1, SW2, SW6 and SW5 are OFF. The flow of current is opposite to the load current. All these modes are shown in fig 3.

3.2 Working of Proposed 17-level Switched Capacitor MLI

The proposed circuit for a 17-level switched capacitor multilevel inverter (SC MLI) is depicted in Figure 4. The circuit comprises a single DC input voltage supply (Vin), twelve switches S_1 to S_{12}, 2 diodes D_1 and D_2, & 3 capacitors C_1, C_2 & C_3. Each switch is accompanied by an anti-parallel diode. This circuit is capable of generating the 17level fourfold boost voltage (0, ± 0.5Vin, ± 1Vin, …, ± 3.5Vin, ± 4Vin) without requiring an H bridge for the change of polarity. The pairs S_1 & S_2 and S_{11} & S_{12} exhibit complementarity when switched, simplifying complexity of control. Similarly, pairs S_5 & S_{10} operate at the fundamental frequency, while S_3 & S_4 are operated at a low frequency, thereby reducing switching losses. Figure 4 also provides a visualization of every switch voltage stress.

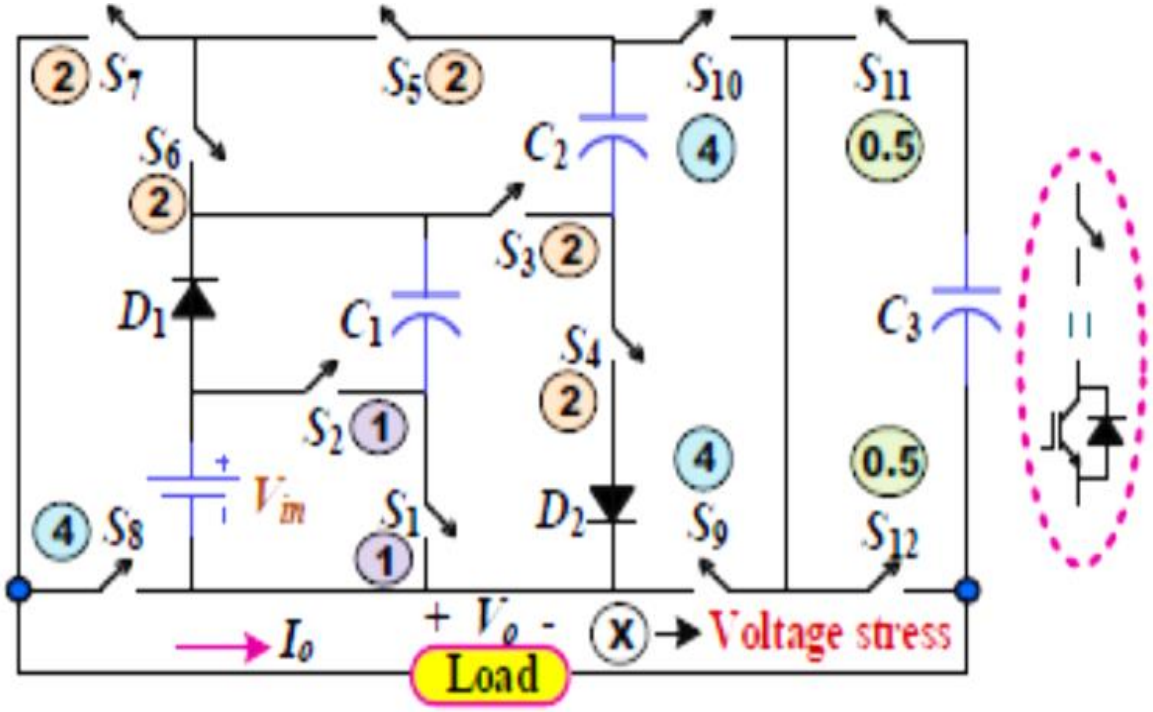


Figure 4: Topology of seventeen level SC MLI [3]

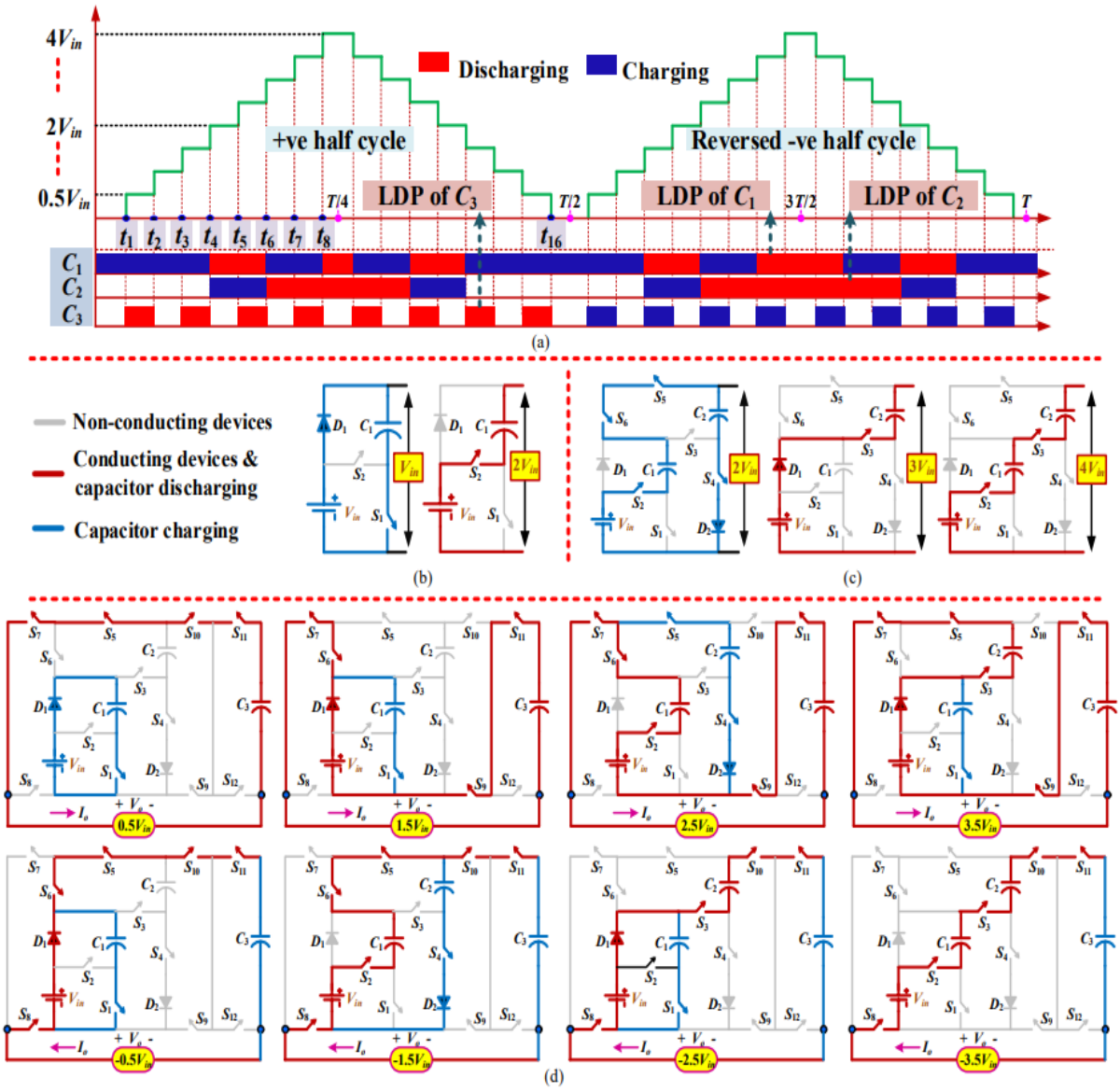


Figure 5:Output waveform of the 17 level SCMLI (a), charging & discharging of capacitors C_1(b), C_2(b) and C_3(d) [3]

During the +ve half of output, the 17-level switched capacitor multilevel inverter (SCMLI) operates as follows: Firstly, capacitor C_3 is discharged, resulting in a voltage step of +0.5Vin. The source voltage is then included in current path of load, where C_3 is bypassed. D_1 conducts forward & switch S_1 clamps output across capacitor(C_1) to Vin, resulting in a second voltage step of +Vin. Additionally, by activating S11, the voltage across C_3 adds to Vin, resulting in +1.5Vin output voltage at the load terminal. C_1 is discharged to the load with V_{in} in series through S_2, while C_2 capacitor is charged with triggering of S_4. To prevent undesired

discharge of capacitor C_2, diode D_2 is connected. The voltage level +2.5Vin & +3.5 Vin is achieved by discharging C_3 which is described earlier. +3 Vin at the load terminal is produced by discharging capacitor C_2 & when C_1, C_2 are discharged in series to input voltage, load voltage becomes + 4Vin.

During the -ve half of output waveform, voltage levels of - Vin, - 2Vin, -3Vin & -4Vin are obtained by triggering S_8, S_{10} and S_{12} but not S_7, S_9 & S_{11} respectively. C_3 is charged to the intermediate voltage steps of -0.5Vin, -1.5Vin, -2.5Vin & -3.5Vin. Importantly, there is always path for flow of current in reverse, ensuring circuit's operation successfully under various power factors of the load.

The required switching patterns to generate the 17 level voltages with different power factor of load are presented in Table 1, while output waveform of the SCMLI with the charging & discharging of capacitors is depicted in fig. 5(a). C_1 is charged in parallel with Vin and is discharged with source in series as shown in fig 5(b). C_2 is charged in with Vin plus V_{C1} in parallel and is discharged in series, providing voltage (2 Vin) at load terminal which is illustrated in fig 5(c). Furthermore, C_3 is discharged during the entire +ve half & symmetrically charged during -ve half of output, thereby + $0.5V_{in}$ is maintained across C_3. Fig 5 (d) provides insight of circuit(equivalent) and path of conduction during different voltage levels in +ve & +ve cycles which confirms balancing capacity of all the three capacitors naturally [3].

Table 1: Switching States of 17 level SCMLI [3]

Conducting switches in Positive half-cycle	Voltage steps	Conducting switches in Negative half-cycle
$S_1 - S_5 - S_7 - S_{10} - S_{12}$	0	$S_1 - S_8 - S_9 - S_{12}$
$S_1 - S_5 - S_7 - S_{10} - S_{11}$	$\pm V_{in}/2$	$S_1 - S_5 - S_6 - S_8 - S_{10} - S_{11}$
$S_1 - S_5 - S_6 - S_7 - S_9 - S_{12}$	$\pm V_{in}$	$S_1 - S_5 - S_6 - S_8 - S_{10} - S_{12}$
$S_1 - S_5 - S_6 - S_7 - S_9 - S_{11}$	$\pm 3V_{in}/2$	$S_2 - S_4 - S_6 - S_8 - S_{10} - S_{11}$
$S_2 - S_4 - S_6 - S_7 - S_9 - S_{12}$	$\pm 2V_{in}$	$S_2 - S_4 - S_6 - S_8 - S_{10} - S_{12}$
$S_2 - S_4 - S_6 - S_7 - S_9 - S_{11}$	$\pm 5V_{in}/2$	$S_1 - S_3 - S_6 - S_8 - S_{10} - S_{11}$
$S_1 - S_3 - S_5 - S_7 - S_9 - S_{12}$	$\pm 3V_{in}$	$S_1 - S_3 - S_6 - S_8 - S_{10} - S_{12}$
$S_1 - S_3 - S_5 - S_7 - S_9 - S_{11}$	$\pm 7V_{in}/2$	$S_2 - S_3 - S_8 - S_{10} - S_{11}$
$S_2 - S_3 - S_5 - S_7 - S_9 - S_{12}$	$\pm 4V_{in}$	$S_2 - S_3 - S_8 - S_{10} - S_{12}$

3.3 Hardware/Software Requirements

3.3.1 Hardware

- Diodes
- Capacitors
- Resistors
- DC Supply
- Oscilloscope
- Multimeter
- Optocoupler MCT2E
- Arduino Uno
- Power MOSFETs: IRFZ44N, IRF9540N
- PCB/ Matrix Board/ Breadboard

3.3.2 Software

- MATLAB/Simulink
- Proteus
- Arduino IDE

3.4 Simulation circuit

The simulation circuit comprises a single DC input voltage supply (Vin), twelve switches S_1 to S_{12}, 2 diodes D_1 and D_2, & 3 capacitors C_1, C_2 & C_3. Each switch is accompanied by an anti-parallel diode. This circuit is capable of generating the 17level fourfold boost voltage (0, ± 0.5Vin, ± 1Vin, …, ± 3.5Vin, ± 4Vin) without requiring an H bridge for the change of polarity. The pairs S_1 & S_2 and S_{11} & S_{12} exhibit complementarity when switched, simplifying complexity of control. Similarly, pairs S_5 & S_{10} operate at the frequency of frequency, while S_3, S_4 are operated at a low frequency, thereby reducing switching losses. Among the switches, only S_8-S_{10} experience the maximum voltage stress at the load. In steady state condition, the voltage ratio across C_1, C_2, C_3 (V_{C1}:V_{C2}:V_{C3}) is maintained 1:2:0.5.

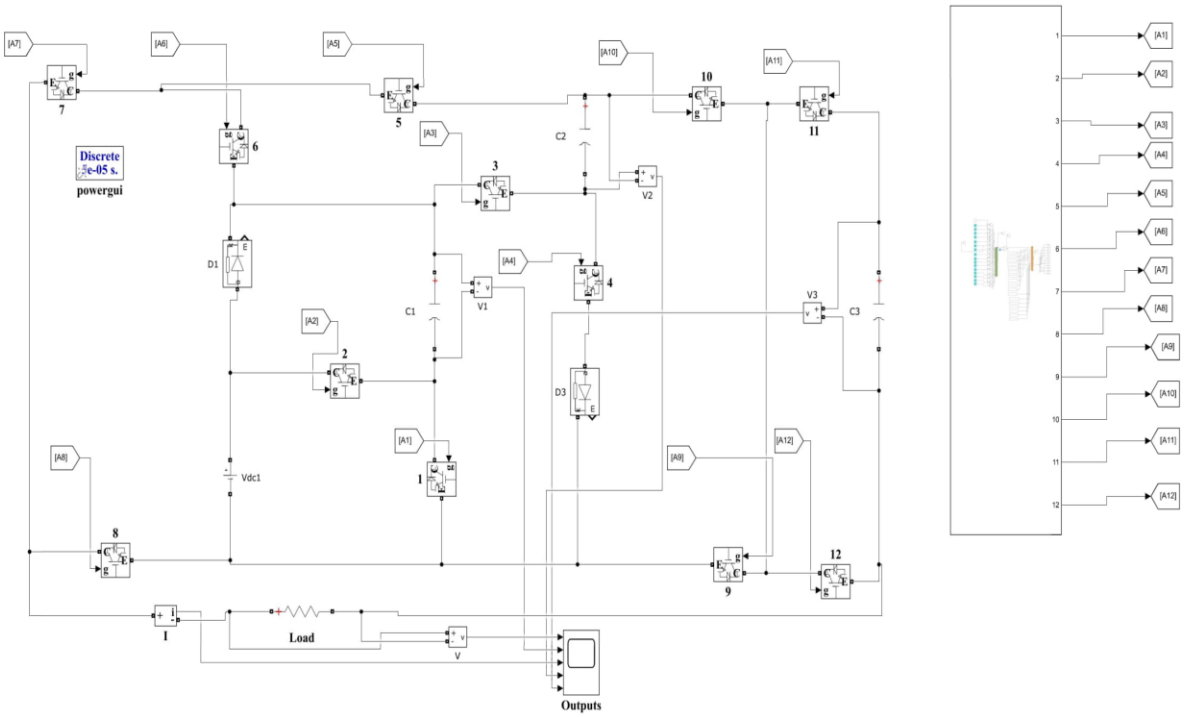


Figure 6: Simulation circuit of single source 17-level SC MLI

The simulated circuit contains a subsystem named “switching circuit” where the switching logics for different switches S_1- S_{12} are implemented. The different switching combinations of switches ensures the various voltage levels across load of resistance 10 ohm. The values of capacitors are calculated as C_1= 3300µF, C_2= 4700µF, C_3= 2200µF. Twelve MOSFETs are used as switches, PWM signals generated from switching circuits are given to the gate of these MOSFETs which enables their switching in different instants of time. As a result, a

multilevel AC signal is obtained at the output. The switching circuit and switching sequence of different switches are shown in figure 7.

Voltage Level (Vout)	s1	s2	s3	s4	s5	s6	s7	s8	s9	s10	s11	s12
-4	0	1	1	0	0	0	0	1	0	1	0	1
-3.5	0	1	1	0	0	0	0	1	0	1	1	0
-3	1	0	1	0	0	1	0	1	0	1	0	1
-2.5	1	0	1	0	0	1	0	1	0	1	1	0
-2	0	1	0	1	0	1	0	1	0	1	0	1
-1.5	0	1	0	1	0	1	0	1	0	1	1	0
-1	1	0	0	0	1	1	0	1	0	1	0	1
-0.5	1	0	0	0	1	1	0	1	0	1	1	0
0	1	0	0	0	1	0	1	1	1	1	0	1
0.5	1	0	0	0	1	0	1	0	0	1	1	0
1	1	0	0	0	1	1	1	0	1	0	0	1
1.5	1	0	0	0	1	1	1	0	1	0	1	0
2	0	1	0	1	0	1	1	0	1	0	0	1
2.5	0	1	0	1	0	1	1	0	1	0	1	0
3	1	0	1	0	1	0	1	0	1	0	0	1
3.5	1	0	1	0	1	0	1	0	1	0	1	0
4	0	1	1	0	1	0	1	0	1	0	0	1

Figure 7: Switching patterns of different switches of 17-level MLI

3.5 Hardware description

After completing simulation of 17 level switched capacitor MLI successfully in MATLAB, we are now dedicated in designing and implementing Multilevel Inverter in hardware. It will be difficult to implement 17-level in hardware (it will require much time and money, not affordable for learning students like us). So, as per suggestion of our supervisor, we will be designing and fabricating 5-level Cascaded H-bridge Multilevel inverter. For the complete design, we need various circuits like DC power supply circuit, driver circuit and inverter circuit.

The components required and circuit diagram for different circuits are explained as follows:

3.5.1 Brief description of components used

1) IRFZ44N

The IRFZ44N is a popular N-channel power MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) that is widely used in a variety of electronic circuits due to its high voltage and current handling capabilities. It is manufactured by International Rectifier, a leading semiconductor company that specializes in power management technologies.

The IRFZ44N is housed in a TO-220 package, which is a commonly used package for discrete power transistors. It features three terminals: the gate (G), the drain (D), and the source (S). The drain and source terminals are used to control the flow of current through the MOSFET, while the gate terminal is used to apply a voltage to control the MOSFET's conductivity.

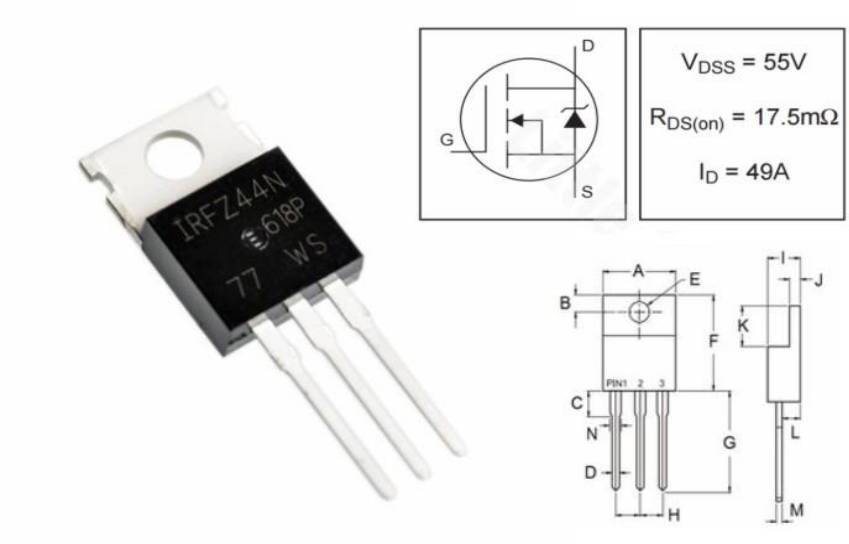


Figure 8: Pinout of IRFZ44N

The key specifications of the IRFZ44N are:

1. Voltage Rating: 55 volts
2. Current Handling Capability: 49 amperes
3. Low On-Resistance: 17 milliohms
4. Gate Threshold Voltage: 2 to 4 volts

5. Fast Switching Speed: The IRFZ44N has a fast-switching speed, with a typical turn-on time (TON) of 14 nanoseconds and a typical turn-off time (TOFF) of 42 nanoseconds, allowing it to be used in applications that require rapid switching.

Overall, the IRFZ44N is a robust and reliable power MOSFET that is widely used in a wide range of electronic circuits due to its high voltage rating, high current handling capability, low on-resistance, low gate threshold voltage, and fast switching speed.

2) IRF9540N

The IRF9540N is a widely used and popular P-Channel power MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) designed for various electronic applications. It is part of the IRF series of power MOSFETs manufactured by Infineon Technologies, a leading semiconductor company.

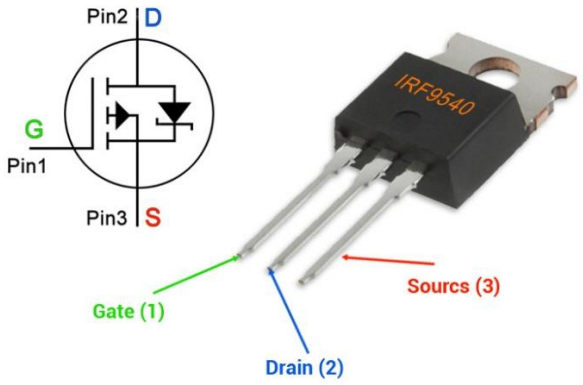


Figure 9: Pinout of IRF9540N

Brief description of the IRF9540N:

1. Power Rating: V_{ds} of -100 volts and a continuous drain current (Id) of -23 amperes.
2. P-Channel MOSFET: The IRF9540N is a P-Channel MOSFET, which means that it conducts current when a negative voltage is applied to the gate terminal. It is designed to be used as a high-side switch, where the load is connected between the drain and the positive supply voltage.
3. Low On-Resistance: R_{ds}(on) of typically 0.17 ohms
4. Fast Switching Speed: The IRF9540N has a fast-switching speed, allowing for efficient switching operations and reducing switching losses. This makes it suitable for applications that require high-frequency switching.

In summary, the IRF9540N is a high-power P-Channel MOSFET with low on-resistance, fast switching speed, and is commonly used in a wide range of applications where efficient high-power switching is required.

3) MCT2E IC: The MCT2E is an optocoupler IC (integrated circuit) that is used to provide electrical isolation between two circuits using an optically coupled interface. It consists of an infrared LED (light-emitting diode) and a phototransistor integrated into a single package.

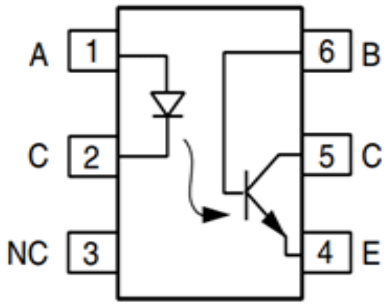


Figure 10: Pinout of MCT2E optocoupler

The MCT2E is commonly used in applications where there is a need to transfer a signal or data between two electrically isolated circuits, while maintaining galvanic isolation to prevent any electrical interference or noise from passing through. This can be useful in situations where there are potential differences, high voltages, or noisy environments that could impact the performance or safety of the circuits.

The MCT2E typically comes in a 6-pin dual-in-line package (DIP), with the following pin configuration:

1. Anode (positive) of the infrared LED, which is used to provide the input signal to be transmitted optically.
2. Cathode (negative) of the infrared LED, which is connected to the ground or reference potential.
3. Emitter of the phototransistor, which is connected to the ground or reference potential.
4. Collector of the phototransistor, which provides the output signal after optically coupling with the input signal.
5. Base of the phototransistor, which is left unconnected or can be used for additional circuitry.
6. No Connection (NC), which is left unconnected.

The MCT2E operates by driving the infrared LED with an input current, which emits infrared light that is then detected by the phototransistor. The phototransistor responds to the intensity of the received light, and its collector-emitter output provides a proportional electrical signal. This output signal is then used to drive the subsequent circuitry, providing electrical isolation between the input and output circuits.

3.5.2 DC power supply

DC power supply is the input signal for the MLI which converts into AC signal. DC power signal can be given by various methods like using rectifier 220/12V, using SMPS using by 12V battery or by DC signal generator. In this project, for testing purposes, we have used battery pack containing 4 cells of 3V each. For obtaining the complete output i.e. full working of inverter, we have used variable DC source from Basic Circuit laboratory of electrical department to produce 12V DC input source for the MLI.

3.5.3 Driver circuit

Driver circuit is required for triggering gate terminal of MOSFET switches that are used in inverter circuit. Optocoupler MCT2E is used in the driver circuit. The pulse width modulation required are given to each gate of MOSFET switches using Arduino uno by coding from Arduino IDE and generated pulse from the driver circuit are given as pulse to trigger gate of MOSFET switches. The inverter circuit for 5 level MLI contains 8 MOSFET switches and each switch requires a driver circuit generating different pulses.

The different components used in the driver circuit are:

- Opto-coupler MCT2E IC
- Arduino Uno
- Resistors 10kohms, 220 ohms, 500ohms
- Power MOSFET IRFZ44N, IRF9540N
- Diode FR107
- Zener diode
- LED

We have connected the components using a breadboard to test the working of driver circuit which is shown is fig 11.

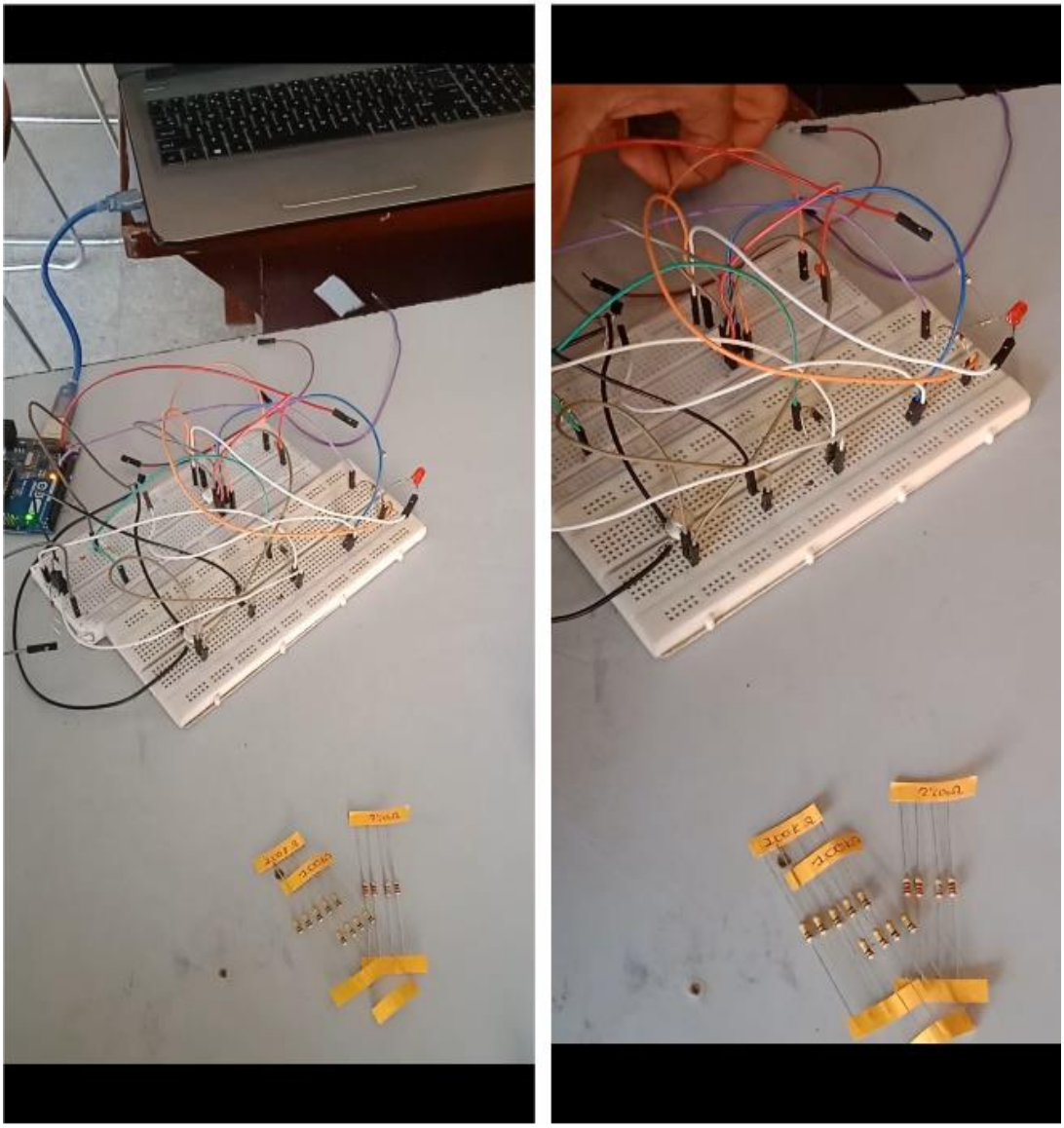


Figure 11: Testing of driver circuit

3.5.4 Inverter Circuit

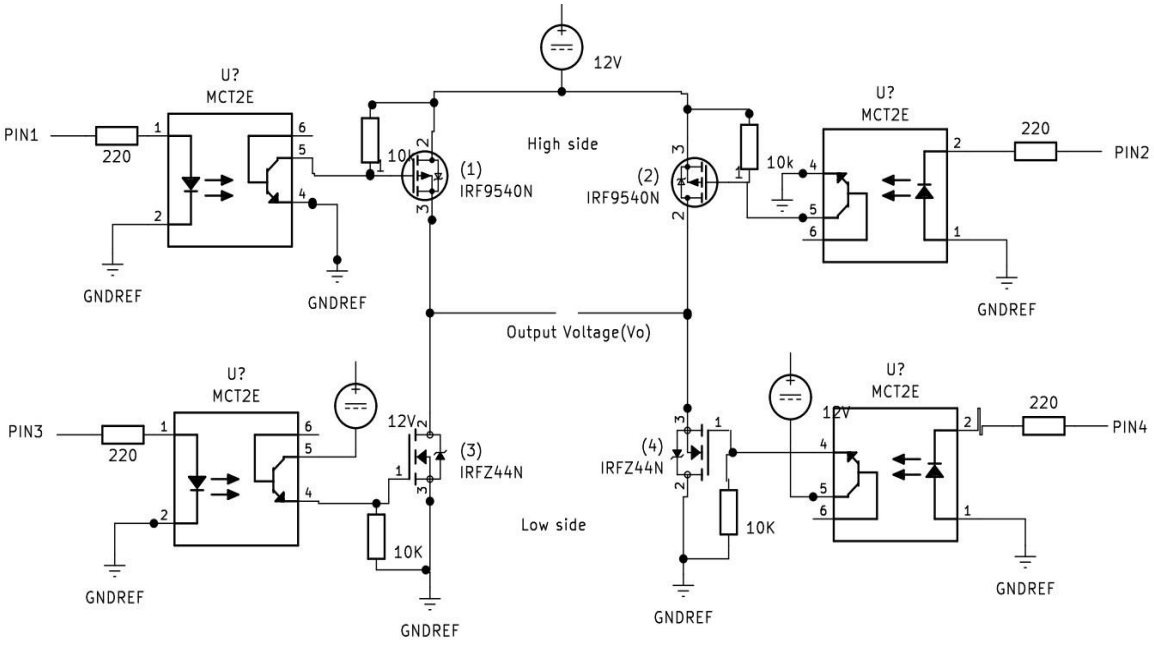


Figure 12: Circuit diagram of single cell H bridge 3 level MLI

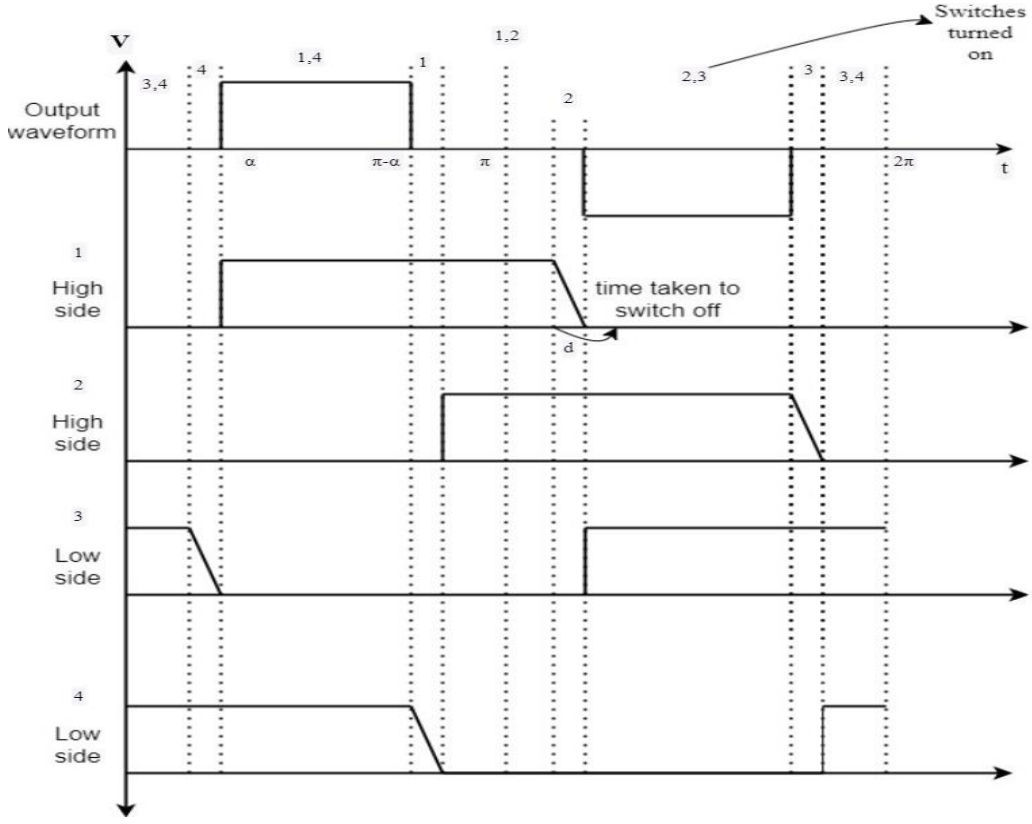


Figure 13: Firing sequence diagram of 3 level H bridge MLI

The inverter circuit for 3 level H bridge Multilevel inverter consists of 4 MOSFETs for producing 3 level of output. 12V DC supply is given to the inverter and optocoupler. The MOSFETs used are: IRFZ44N, a N-channel MOSFET (for low side switching) and IRF9540N, a P-channel MOSFET (for high side switching). Gate terminal of each MOSFETs is triggered by a driver circuit that consists of MCT2E optocoupler. PWM for each gate is generated by appropriate coding using Arduino IDE and is given to Pin 1,2,3,4 of driver circuit as shown in the circuit diagram above.

The circuit diagram of 3 level H bridge MLI is shown in fig 15. If two H bridges are cascaded in series, 5 level cascaded H bridge is formed. The hardware implementation of 5 level CHB MLI is shown in fig 16.

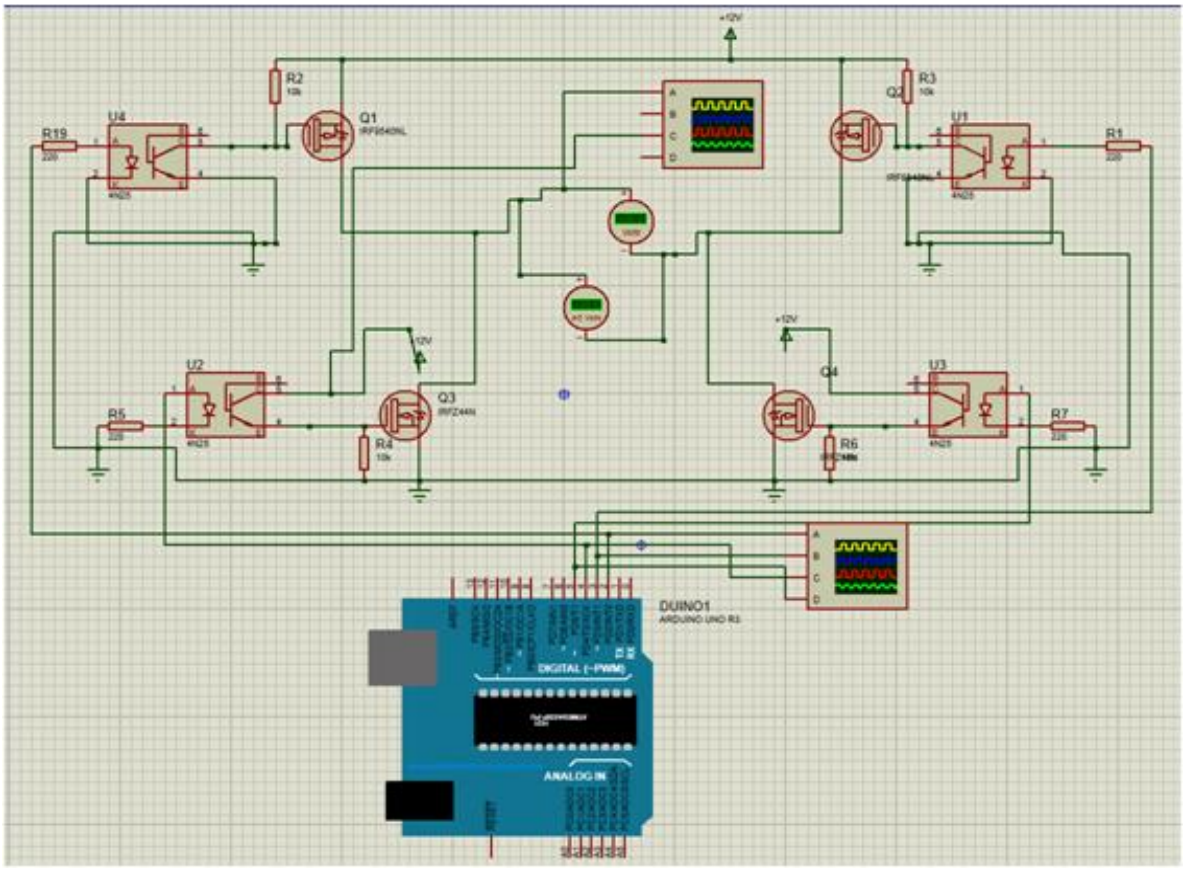


Figure 14: Circuit diagram of 3 level H bridge MLI in proteus

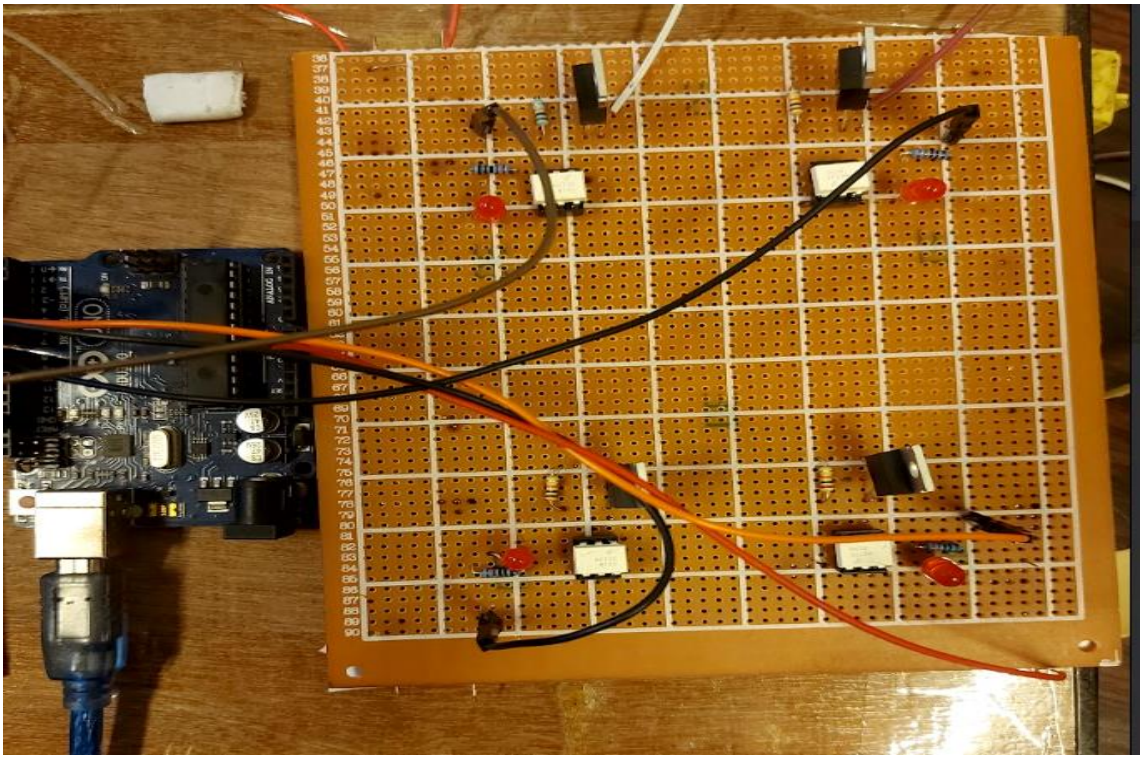


Figure 15: Hardware implementation of 3 level H bridge MLI

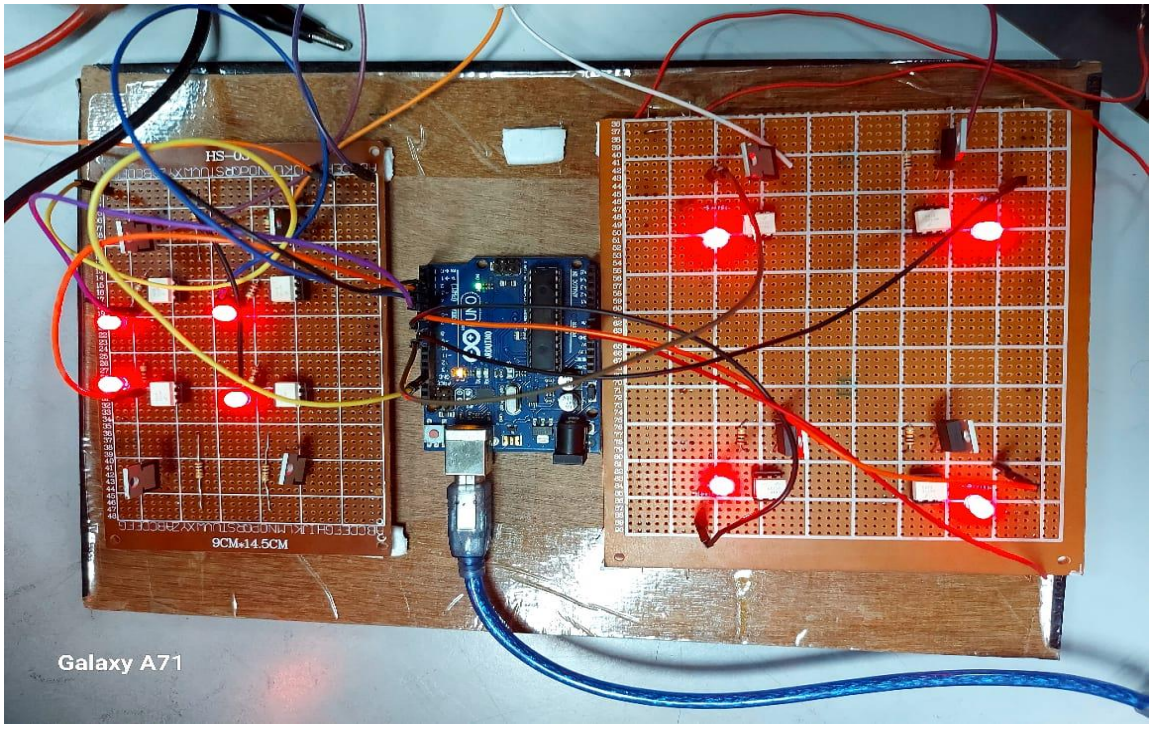


Figure 16: Hardware implementation of 5 level CHB MLI

CHAPTER FOUR
RESULT AND DISCUSSION

4.1 5-level cascaded H-bridge MLI

The simulation circuit of 5-level cascaded MLI is shown in appendix fig 27A. Output voltage waveform of 5-level cascaded H-bridge MLI Output voltage waveform of 5-level cascaded H-bridge MLI is shown in fig 17.

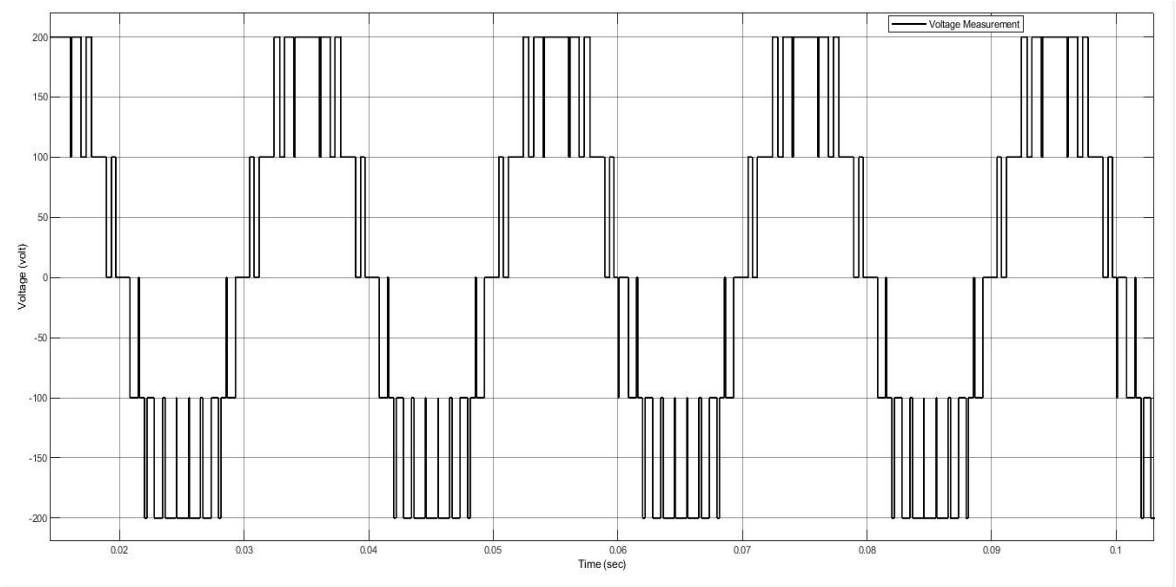


Figure 17: Output voltage waveform of 5-level cascaded H-bridge MLI

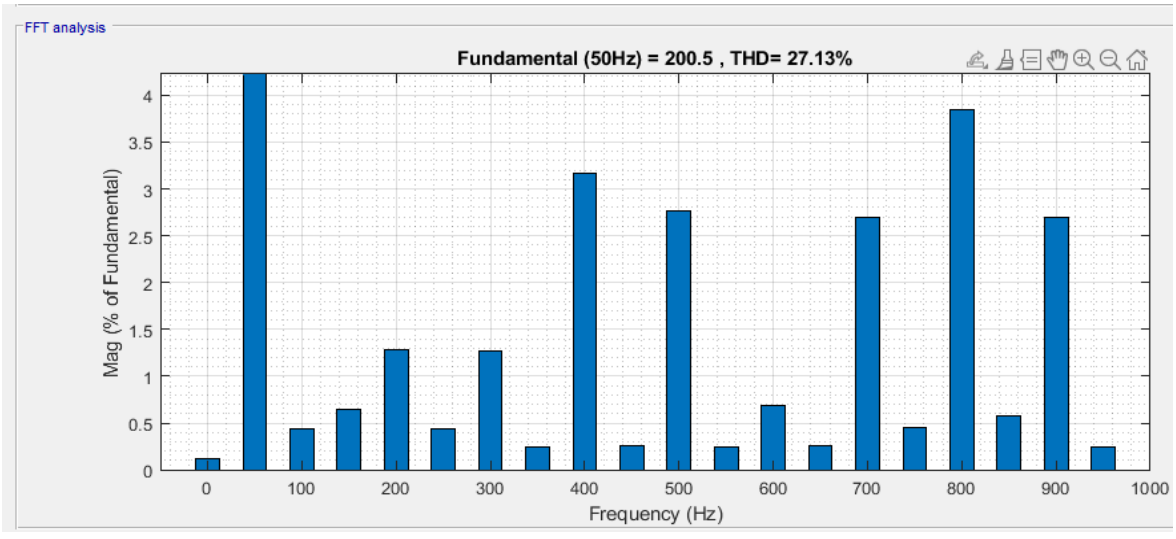


Figure 18:THD of 5-level cascaded H-bridge MLI

The Total Harmonic Distortion (THD) level of 5-level cascaded H-bridge MLI was obtained as shown in fig 18. The THD was obtained 27.13% which comes very close to the THD level according to IEEE standards i.e. 27.2%.

4.2 9-level cascaded H-bridge MLI

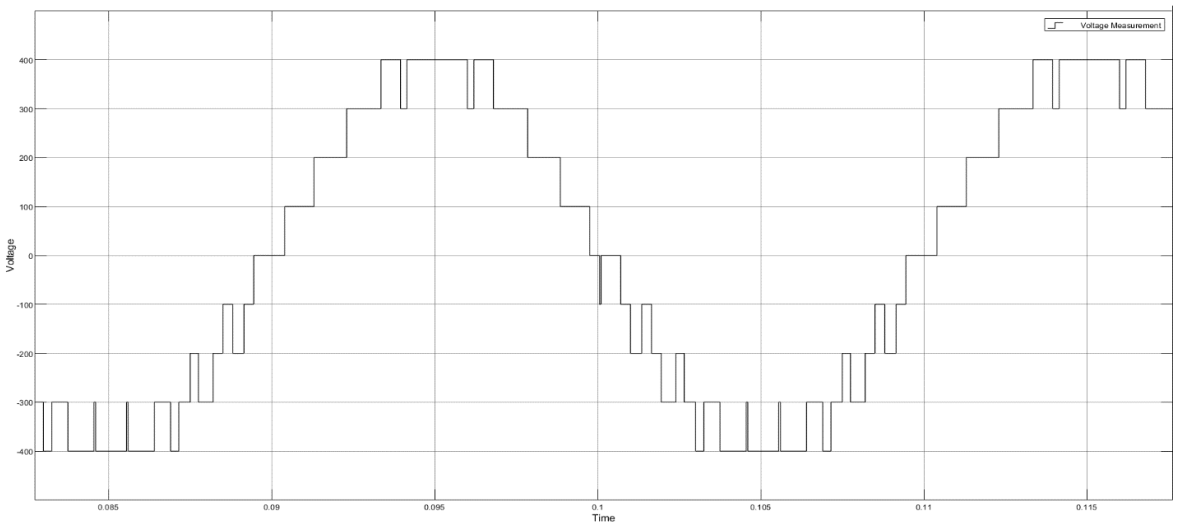


Figure 19:Output voltage waveform of 9-level cascaded H-bridge MLI

The output of 9-level cascaded H-bridge MLI was obtained as shown in fig 19. The output waveform resembles more to sinusoidal waveform as compared to 5-level cascaded H-bridge MLI. This means as the number of levels of output waveform is increased, the output becomes more sinusoidal AC which contains less harmonics.

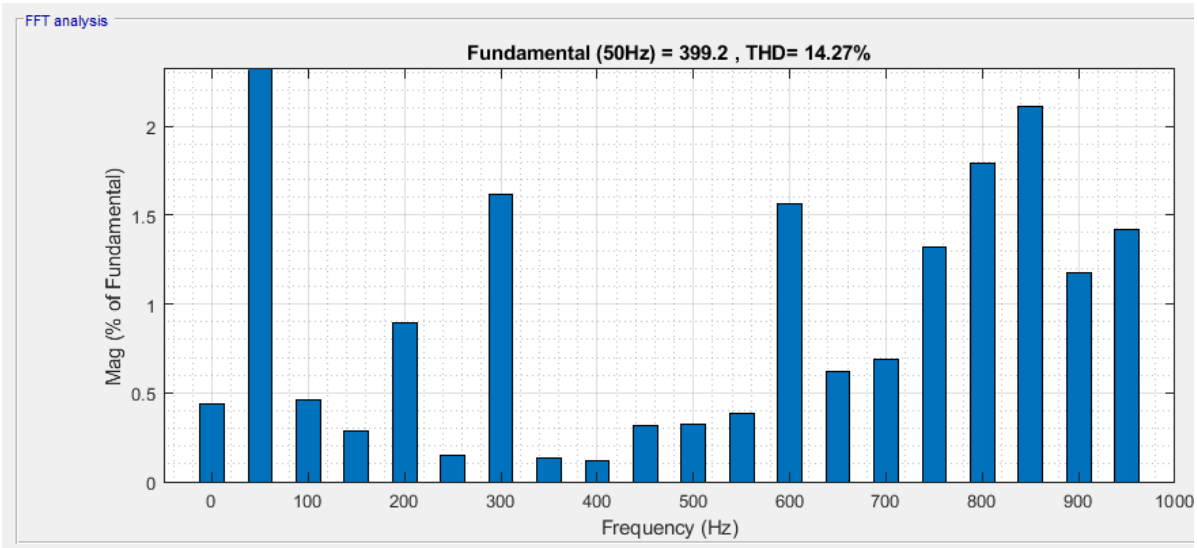


Figure 20:THD of 9-level cascaded H-bridge MLI

Similarly, the THD level of 9-level cascaded H-bridge MLI was obtained as shown in fig 20. The output waveform resembles more to sinusoidal waveform as compared to 5-level cascaded H-bridge MLI. The THD was obtained 14.27% which comes very close to the THD level according to IEEE standards i.e.14.18%.

4.3 9-level switched capacitor cascaded H-bridge MLI

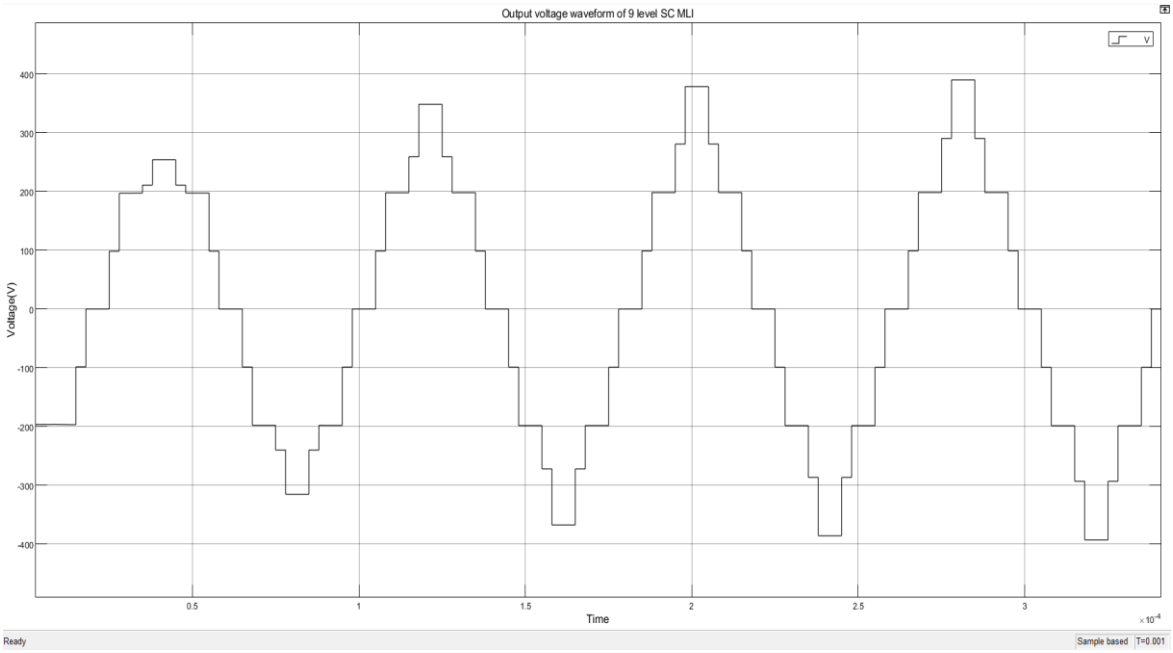


Figure 21:Output voltage waveform of 9-level switched capacitor CHB MLI

The output of 9-level SC CHB MLI was obtained as shown in fig 21. The output waveform resembles more to sinusoidal waveform as compared to 5-level cascaded H-bridge MLI. The number of components used in this topology is less and hence losses are reduced thus increasing quality of output. Due to charging of capacitor, output voltage is increasing at the start but it saturates and produces a continuous periodic waveform after some instant of time.

4.4 17-level Switched capacitor Multilevel Inverter

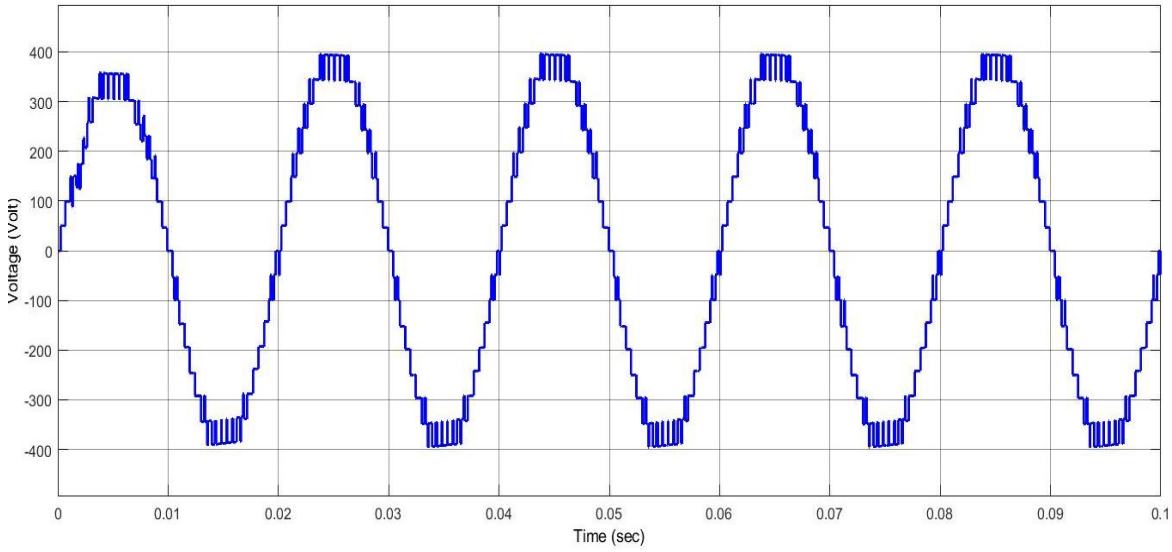


Figure 22:Output voltage waveform of single source 17-level SC MLI

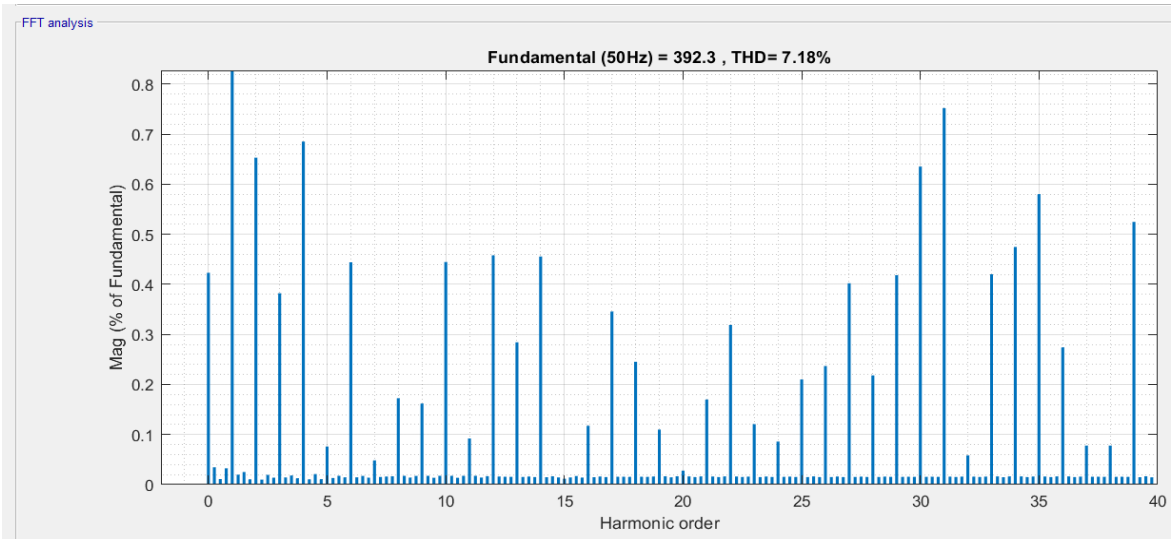


Figure 23:Total Harmonic Distortion (THD) calculation of single source 17-level SC MLI

The output of a single source 17-level SC MLI was obtained as shown in fig 23. The output waveform resembles more to sinusoidal waveform as compared to 9-level cascaded H-bridge MLI. To produce a 17-level output waveform, there will be many switches and components used due to which there are more switching losses, ripple losses and conduction losses. The number of components used in this topology is less. Hence, losses are reduced thus increasing

quality of output. Due to charging of capacitor, the output voltage is increasing at the start but it saturates and produces a continuous periodic waveform after some instant of time. The voltage is raised upto 4 times than input voltage (V_{in}) without using DC-DC converter. The input voltage was 100V and output voltage was observed 400V. The THD was also calculated and it was found that THD=7.18% was reduced more significantly in 17-level SC MLI.

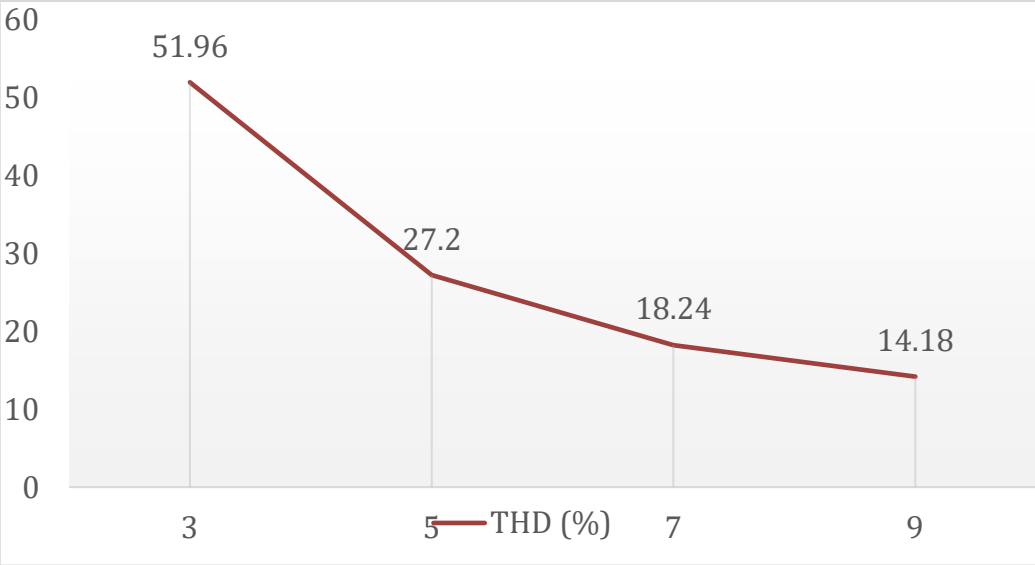


Figure 24: THD vs Levels of inverter

Table 2: MLI levels and THD

Levels of MLI	Cascaded H bridge type, THD level (%)	Switched capacitor type. THD level (%)	IEEE THD level (%)
5	27.13	27.09	27.2
9	14.27	14.21	14.18
17	7.22	7.18	7.11

As seen from fig 24 and table 2, increasing number of levels of MLI decreases THD level and the output voltage waveform becomes more and more sinusoidal. Similarly, use of Switched capacitor topology of MLI also decreases THD than that of H bridge type of same level. Thus, it is more advantageous to use Switched capacitor type multilevel inverter.

4.5 Output of 3 level MLI in hardware

Figure 25: Output waveform of 3 level H bridge MLI

The output waveform of single cell H bridge multilevel inverter is shown in fig 25. The results obtained are:

- Output voltage: 48.7V (peak to peak) which is 2 times than the supply voltage.
- Output frequency: 49.423 Hz which is very close to standard AC frequency 50Hz

Due to absence of THD meter, we were not able to measure the total harmonic distortion of the output waveform. Also, the waveform wasn't smooth enough and contains some glitches due to some losses in the circuit.

4.6 Output of 5 level CHB MLI in hardware

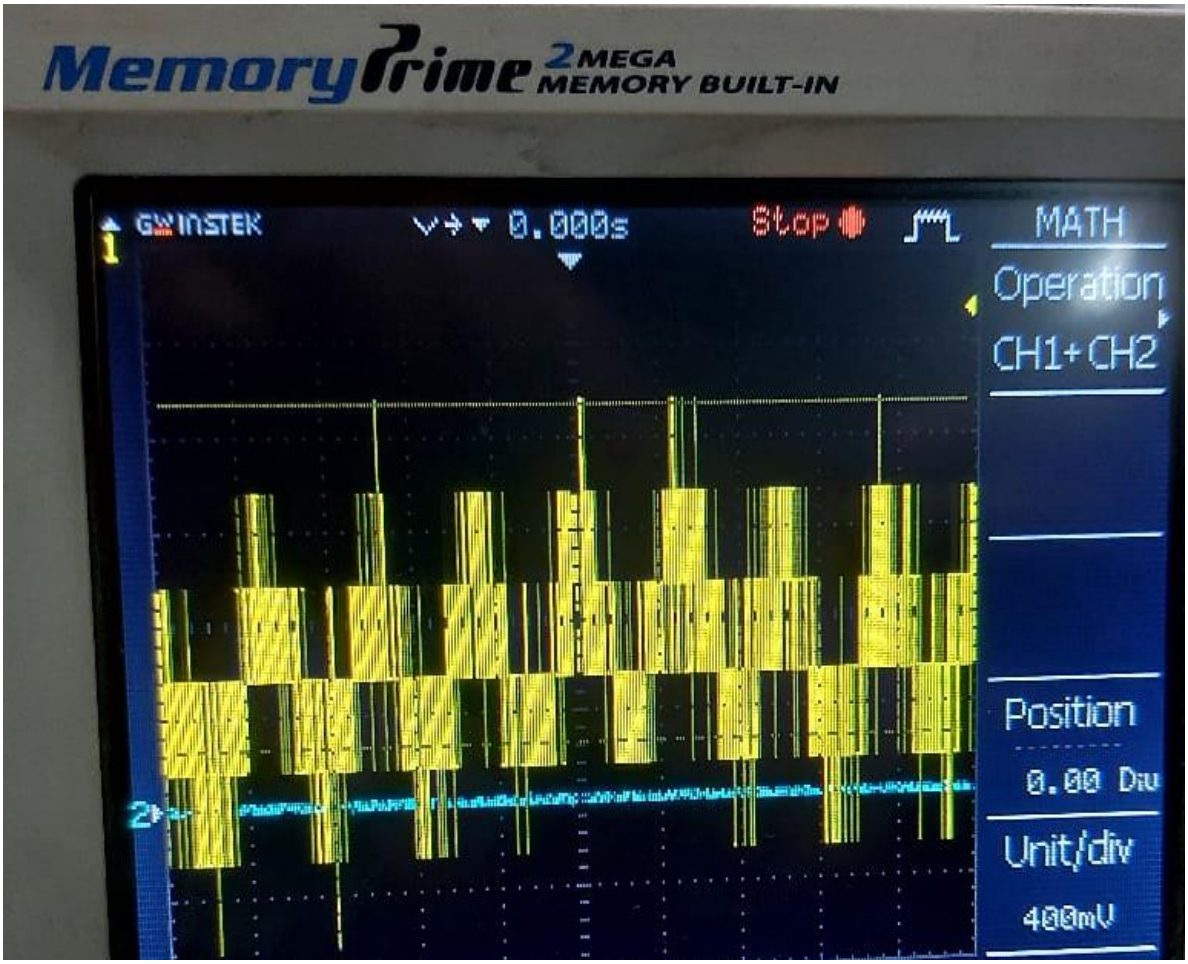


Figure 26: Output waveform of 5 level CHB MLI

The output waveform of 5 level cascaded H bridge MLI in hardware is seen using a digital oscilloscope in the lab. The 5-level waveform is shown in fig 26. It is not too perfect due to some losses (heating losses, leakage current) in the circuit. Due to absence of THD meter in the laboratory, we were not able to measure the total harmonic distortion of the output waveform.

CHAPTER FIVE
CONCLUSION AND RECOMMENDATION

5.1 CONCLUSION

After conducting MATLAB simulations of Cascaded Multilevel Inverter and Switched Capacitor Multilevel Inverter up to 17 level, the hardware implementation of 3 & 5 level CHB MLI is done. The hardware setup is divided into three sections: the DC power supply, driver circuit, and inverter circuit. The output voltage waveform of different multilevel topologies is obtained and analyzed. The THD obtained are: 27.13% for 5 level CHB MLI, 14.27% for 9 level CHB MLI, 14.21% for 9 level SC MLI and 7.18% for 17 level SC MLI. Multilevel inverters offer several advantages such as high-quality power, reduced harmonic distortion, suitability for high-power applications, and decreased switching losses. They find applications in various fields including UPS, high voltage DC transmission, variable frequency drives, pumps, and conveyors. However, challenges are arisen due to the complexity of PWM signal generation for MOSFET gate control and the elevated thermal temperatures resulting from high-speed switching. The research is focused on making the hardware more efficient, compact, and cost-effective. Throughout the project, valuable insights of various topics such as power electronic devices, Pulse Width Modulation, different multilevel inverter topologies, and Total Harmonic Distortion are gained.

5.2 RECOMMENDATIONS

- The future scope of the project can be implemented with higher MLI by connecting many numbers of H Bridge in series thereby decreasing the THD of output wave.
- We can also use filtering circuitry at the output terminals to remove harmonics and further reduce THD of the output waveform.
- Switched capacitor topology can be implemented which contains lesser components and less DC sources.

REFERENCES

[1] N. Sandeep and U. R. Yaragatti, "A Switched-Capacitor-Based Multilevel Inverter Topology With Reduced Components," IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5538–5542, Jul. 2018.

[2] E. Babaei, M. Farhadi Kangarlu, and M. Sabahi, "Extended multilevel converters: an attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters," *IET Power Electronics*, vol. 7, no. 1, pp. 157–166, Jan. 2014.

[3] E. Babaei and S. S. Gowgani, "Hybrid Multilevel Inverter Using Switched Capacitor Units," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4614–4621, Sep.2014

[4] T. Roy and P. K. Sadhu, "A Step-up Multilevel Inverter Topology Using Novel Switched Capacitor Converters with Reduced Components," *IEEE Transactions on Industrial Electronics* 2020.

[5] P. Palanivel, S.S. Dash, Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques. IET Power Electron. 4(8), 951–958 (2011)

[6] A.K. Panda, Y. Suresh, Research on cascaded multilevel inverter with single DC source by using three-phase transformers. Electr. Power Energy Syst. 409–420 (2012)

[7] P. R. Bana, K. P. Panda, and G. Panda, "Power Quality Performance Evaluation of Multilevel Inverter With Reduced Switching Devices and Minimum Standing Voltage," IEEE Transactions on Industrial Informatics, vol. 16, no. 8, pp. 5009–5022, Aug. 2020.

[8] M. di Benedetto, A. Lidozzi, L. Solero, F. Crescimbini, and P. J. Grbović, "Five-Level E-Type Inverter for Grid-Connected Applications," IEEE Transactions on Industry Applications, vol. 54, no. 5, pp. 5536–5548, Sep. 2018.

[9] S. S. Lee, B. Chu, N. R. N. Idris, H. H. Goh, and Y. E. Heng, "Switched-Battery Boost-Multilevel Inverter with GA Optimized SHEPWM for Standalone Application," IEEE Transactions on Industrial Electronics, vol. 63, no. 4, pp. 2133–2142, Apr. 2016.

[10] L. Wang, Q. H. Wu, and W. Tang, "Novel Cascaded Switched-Diode Multilevel Inverter for Renewable Energy Integration," IEEE Transactions on Energy Conversion, vol. 32, no. 4, pp. 1574–1582, Dec. 2017.

[11] N. Sandeep and U. R. Yaragatti, “Operation and Control of an Improved Hybrid Nine-Level Inverter,” IEEE Transactions on Industry Applications, vol. 53, no. 6, pp. 5676–5686, Nov. 2017.

[12] P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, “Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation,” IEEE Access, vol. 7, pp. 54888–54909, 2019.

APPENDIX

APPENDIX A (Simulation circuits)

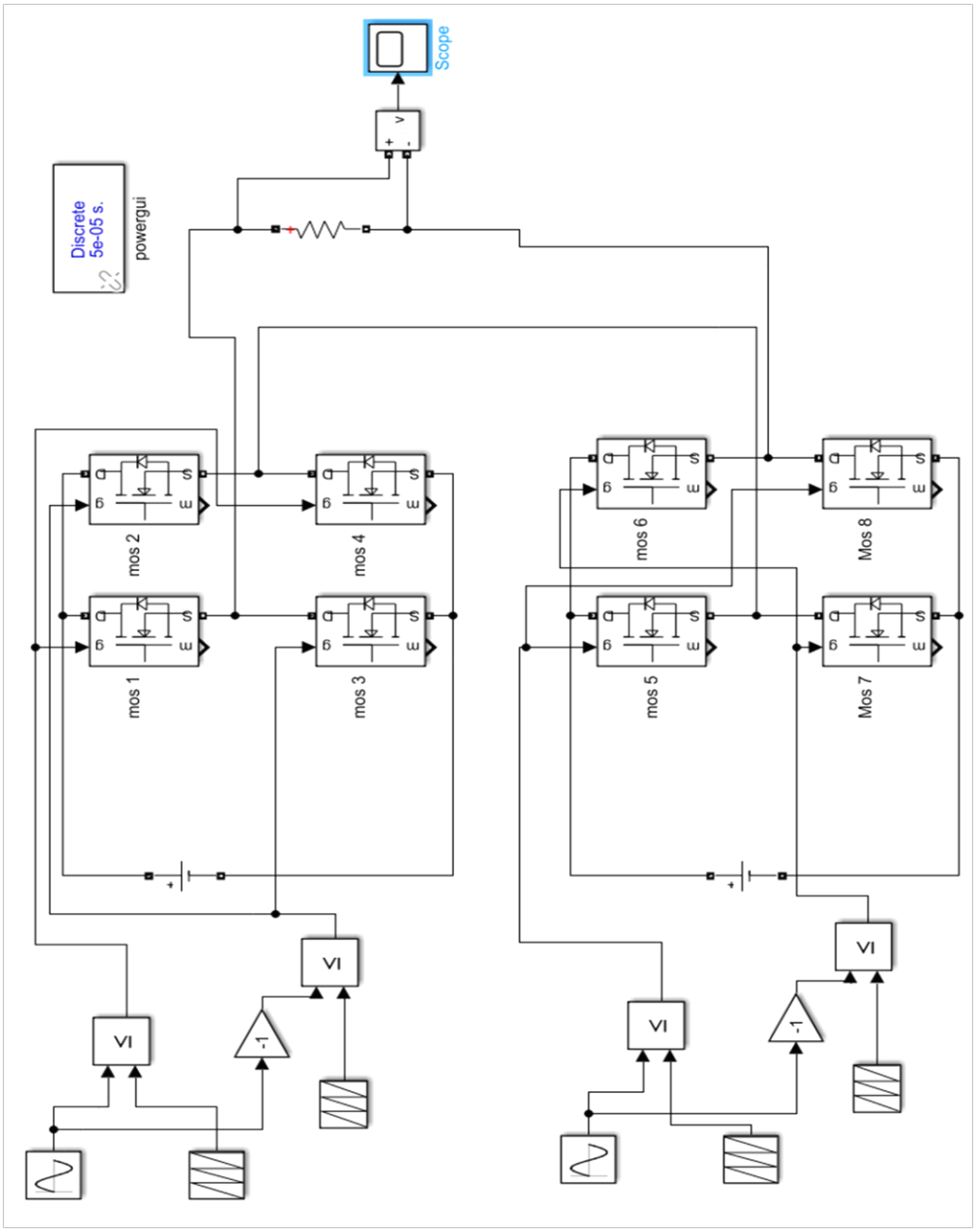


Figure 27A: Simulation circuit of 5-level cascaded H-bridge MLI

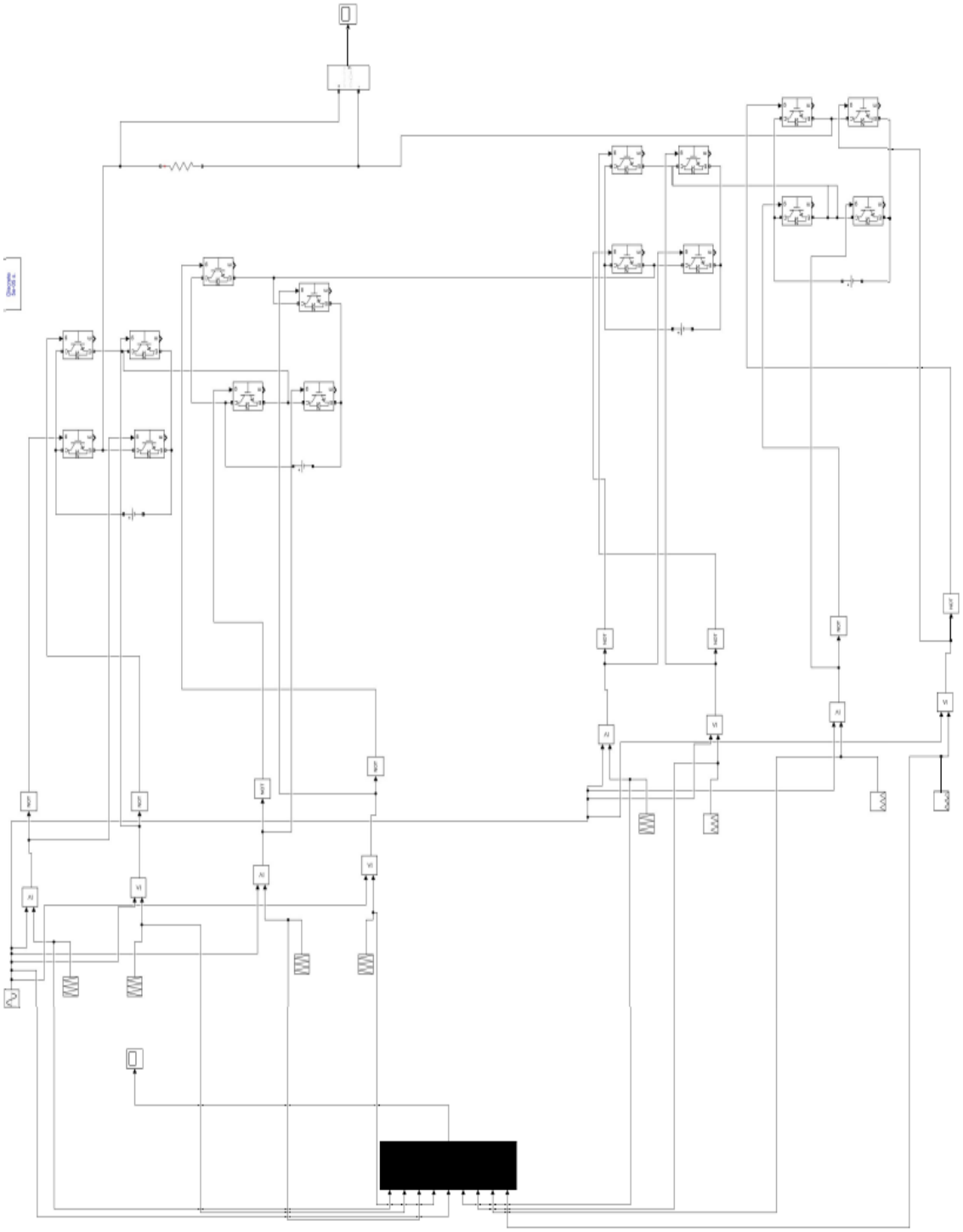


Figure 28A: Simulation circuit of cascaded H bridge 9 level MLI

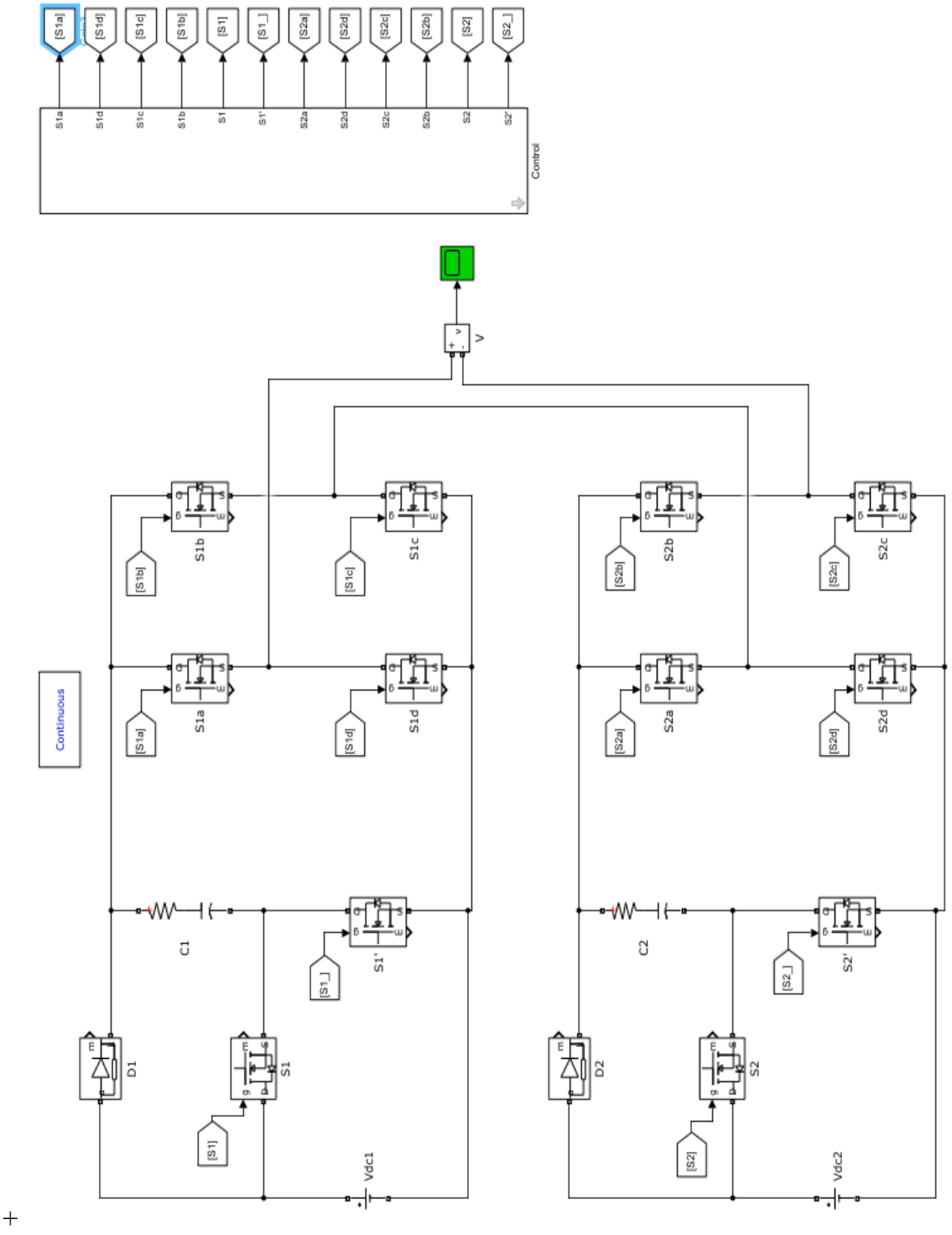


Figure 29A: Simulation circuit of 9-level switched capacitor cascaded H-bridge MLI

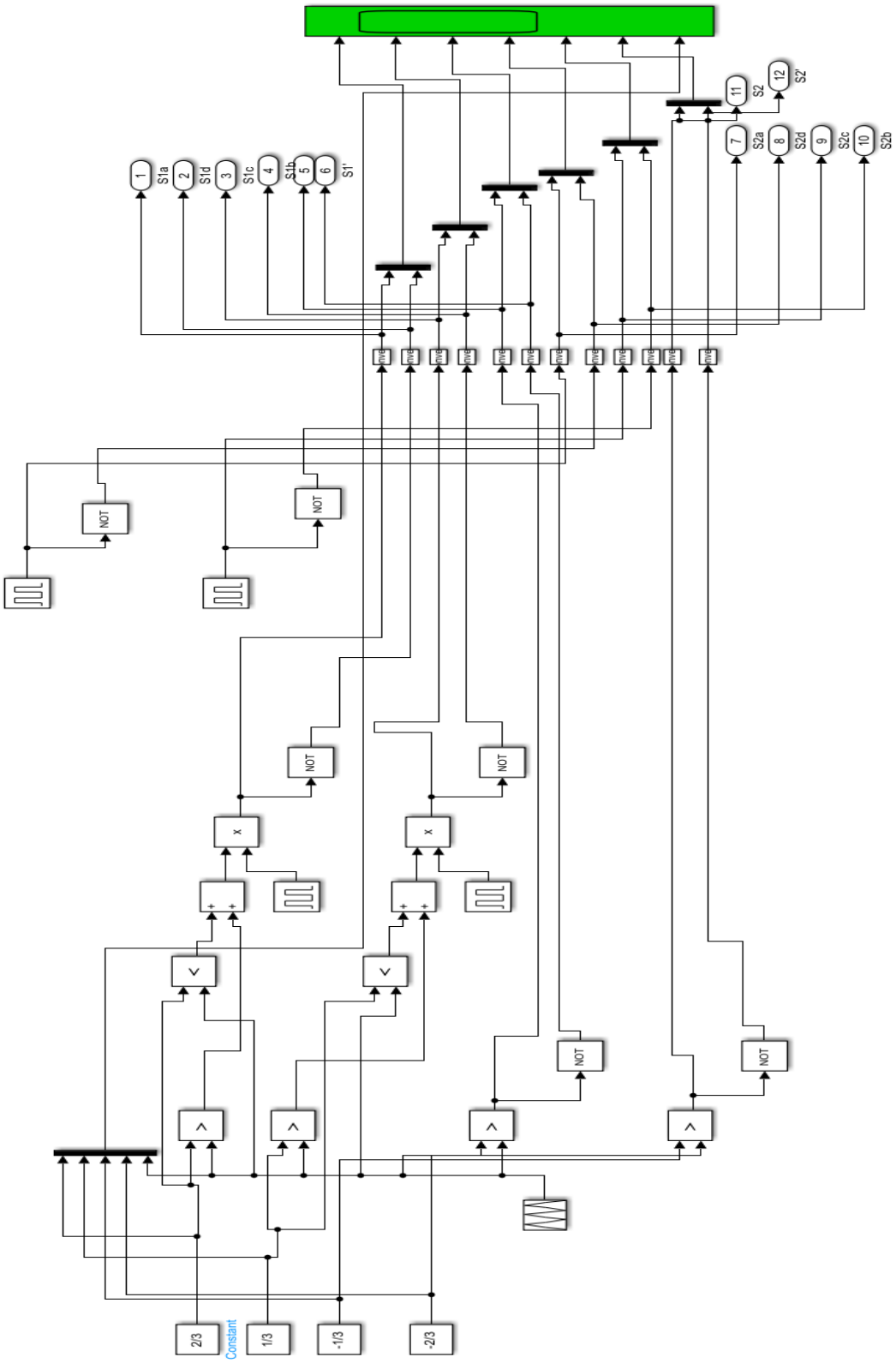


Figure 30A: Control circuit of switched capacitor 9 level MLI

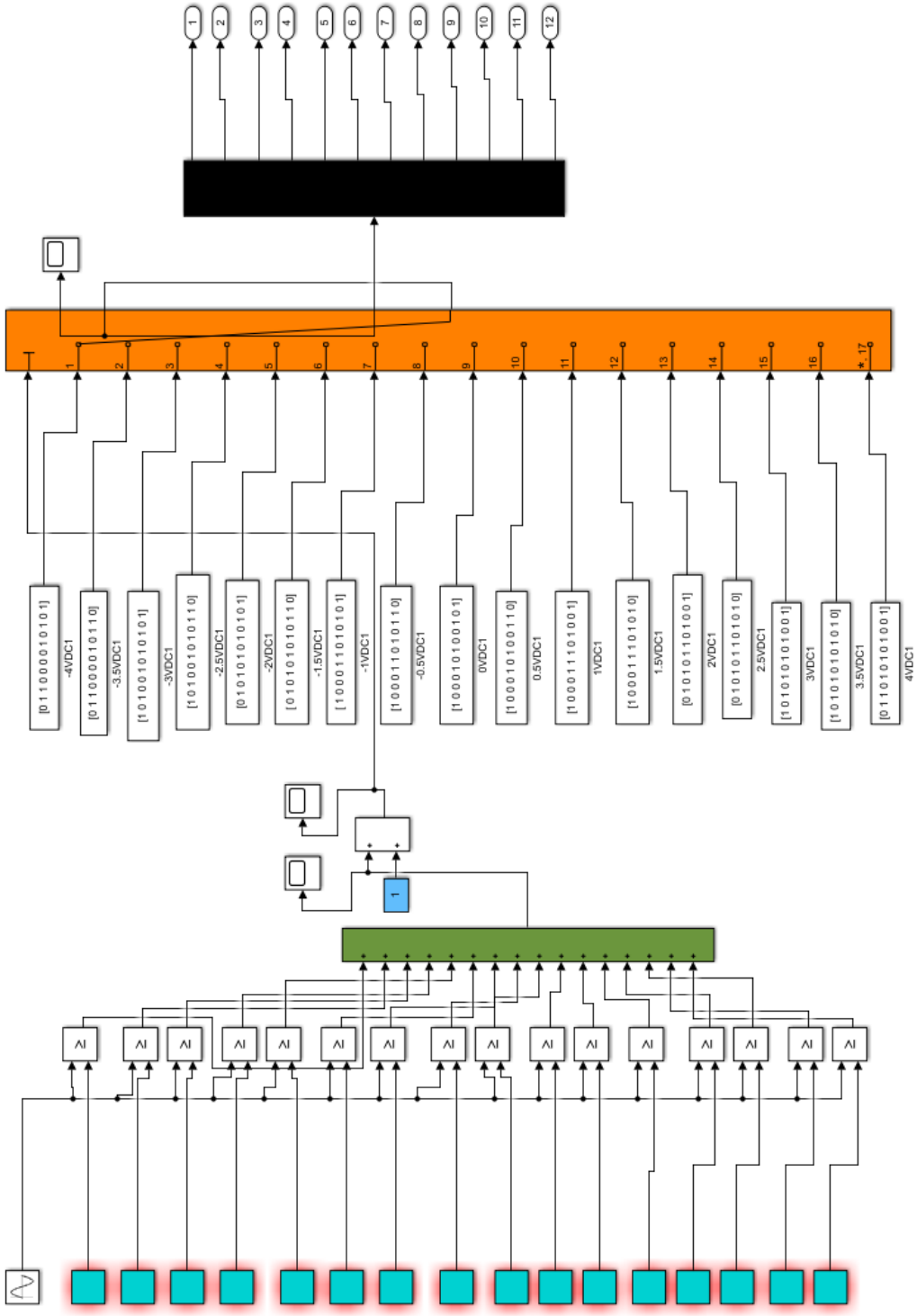


Figure 31A: Switching circuit of 17-level SC MLI

APPENDIX B (Arduino Code)

Arduino code for generating PWM for 3 level inverter

```
float f=50;
float t=(1/f)*1000000;
float a1=45;
float a1p1=(a1*t)/360;
float d=5;

int pin1=3;
int pin2=5;
int pin3=6;
int pin4=9;
void setup(){
  pinMode(pin1, OUTPUT);
  pinMode(pin2, OUTPUT);
  pinMode(pin3, OUTPUT);
  pinMode(pin4, OUTPUT);
}
void loop(){
  digitalWrite(pin3,HIGH);
  delayMicroseconds(a1p1);
  digitalWrite(pin4,HIGH);
  delayMicroseconds(a1p1);
  digitalWrite(pin3, LOW);
  delayMicroseconds(d);
  digitalWrite(pin1,HIGH);
  delayMicroseconds(t/2-(2*a1p1)-d);
  digitalWrite(pin4,LOW);
  delayMicroseconds(d);
  digitalWrite(pin2, HIGH);
  delayMicroseconds((2*a1p1)-d);
```

```
  digitalWrite(pin1,LOW);
  delayMicroseconds(d);
  digitalWrite(pin3,HIGH);
  delayMicroseconds(t/2-(2*a1p1)-d);

   digitalWrite(pin2,LOW);
   delayMicroseconds(d);
   digitalWrite(pin4,HIGH);
   delayMicroseconds((2*a1p1)-d);
}
```

Arduino code for generating PWM for 5 level inverter

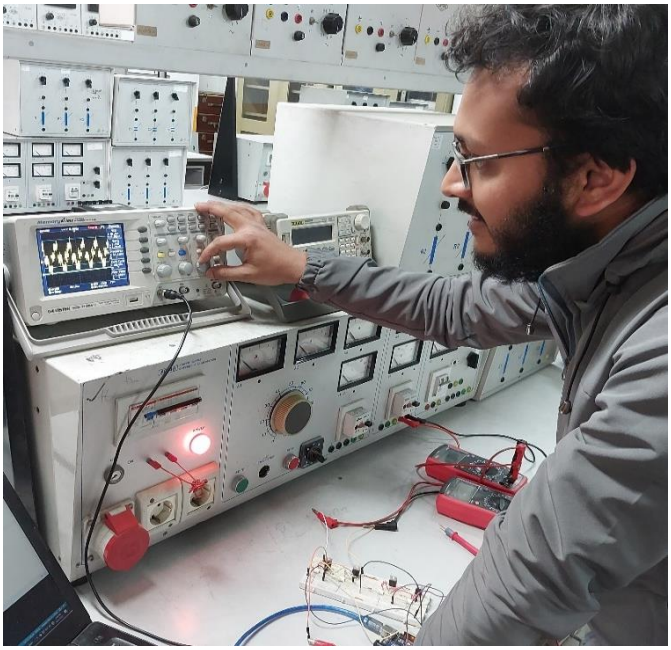
```
float f=50;
float t=(1/f)*1000000;
float a1=10;
float a2=40;
float alp1=(a1*t)/360;
float alp2=(a2*t)/360;
float d=5;

int pin1=1;
int pin2=2;
int pin3=3;
int pin4=4;
int pin5=5;
int pin6=6;
int pin7=7;
int pin8=8;
void setup() {
  pinMode(pin1, OUTPUT);
  pinMode(pin2, OUTPUT);
```

```
  pinMode(pin3, OUTPUT);
  pinMode(pin4, OUTPUT);
  pinMode(pin5, OUTPUT);
  pinMode(pin6, OUTPUT);
  pinMode(pin7, OUTPUT);
  pinMode(pin8, OUTPUT);
  }

void loop() {
digitalWrite(pin1, HIGH);
digitalWrite(pin2, HIGH);
digitalWrite(pin5, HIGH);
digitalWrite(pin6, HIGH);
    delayMicroseconds(alp1-d);

digitalWrite(pin2, LOW);
    delayMicroseconds(d);
digitalWrite(pin4, HIGH);
    delayMicroseconds(alp2-alp1-d);

digitalWrite(pin6, LOW);
    delayMicroseconds(d);
digitalWrite(pin8, HIGH);
    delayMicroseconds(t/2-(2*alp2)-d);

digitalWrite(pin5, LOW);
    delayMicroseconds(d);
digitalWrite(pin7, HIGH);
    delayMicroseconds(alp2-alp1-d);

digitalWrite(pin1, LOW);
```

```
    delayMicroseconds(d);
digitalWrite(pin3, HIGH);
    delayMicroseconds((2*alp1)-d);

 digitalWrite(pin4, LOW);
    delayMicroseconds(d);
digitalWrite(pin2, HIGH);
    delayMicroseconds(alp2-alp1-d);

 digitalWrite(pin8, LOW);
    delayMicroseconds(d);
digitalWrite(pin6, HIGH);
    delayMicroseconds(t/2-(2*alp2)-d);

  digitalWrite(pin7, LOW);
    delayMicroseconds(d);
digitalWrite(pin5, HIGH);
    delayMicroseconds(alp2-alp1-d);

  digitalWrite(pin3, LOW);
    delayMicroseconds(d);
digitalWrite(pin1, HIGH);
    delayMicroseconds(alp1);
    }
```

APPENDIX C (Gallery)

Some glimpses of our team working in the project.



MLI

ORIGINALITY REPORT

16%
SIMILARITY INDEX

PRIMARY SOURCES

1	wrap.warwick.ac.uk Internet	109 words — 2%
2	M. Jagabar Sathik, Kaustubh Bhatnagar, Yam P. Siwakoti, Hussain M. Bassi et al. "Switched-capacitor multilevel inverter with self-voltage-balancing for high-frequency power distribution system", IET Power Electronics, 2020 Crossref	73 words — 1%
3	Usha Sengamalai, T. M. Thamizh Thentral, Palanisamy Ramasamy, Mohit Bajaj et al. "Mitigation of Circulating Bearing Current in Induction Motor Drive Using Modified ANN Based MRAS for Traction Application", Mathematics, 2022 Crossref	45 words — 1%
4	"Innovations in Electrical and Electronics Engineering", Springer Science and Business Media LLC, 2020 Crossref	41 words — 1%
5	Ronak A. Rana, Sujal A. Patel, Anand Muthusamy, Chee woo Lee, Hee-Je Kim. "Review of Multilevel Voltage Source Inverter Topologies and Analysis of Harmonics Distortions in FC-MLI", Electronics, 2019 Crossref	39 words — 1%

6	www.freepatentsonline.com Internet	36 words — 1%
7	www.homemade-circuits.com Internet	28 words — < 1%
8	S. Ranjan, S. K. Mishra. "Analysis of asymmetrical cascaded multilevel inverter for traction systems", 2013 International Conference on Energy Efficient Technologies for Sustainability, 2013 Crossref	23 words — < 1%
9	Sabari, A., R. Omar, M. Sulaiman, and M. Rasheed. "Optimization and Non-Optimization of H-Bridge Cascaded Multilevel Inverter", 3rd IET International Conference on Clean Energy and Technology (CEAT) 2014, 2014. Crossref	23 words — < 1%
10	Marian K. Kazimierczuk. "Pulse - Width Modulated DC - DC Power Converters", Wiley, 2008 Crossref	22 words — < 1%
11	Sun, Xing-tao, and Sheng-wei Gao. "Research on topology and PWM control method of a novel cascaded multilevel inverter", 2010 IEEE International Conference on Mechatronics and Automation, 2010. Crossref	22 words — < 1%
12	hdl.handle.net Internet	22 words — < 1%
13	webfiles.portal.chalmers.se Internet	22 words — < 1%
14	Régis Chayramy, Steven Yang, Oliver Power, Stephane Solve. "Metrology of zener-based	21 words — < 1%

secondary voltage standards", Measurement Science and Technology, 2021
Crossref

15 eprints.lib.hokudai.ac.jp
Internet
18 words — < 1%

16 B.M. Han, S.I. Moon. "Static reactive-power compensator using soft-switching current-source inverter", IEEE Transactions on Industrial Electronics, 2001
Crossref
16 words — < 1%

17 Kaibalya Prasad Panda, Prabhat Ranjan Bana, Gayadhar Panda. "Reduced Switch Count Seven-level Self-Balanced Switched-Capacitor Boost Multilevel Inverter", 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 2020
Crossref
16 words — < 1%

18 Mohammad Mardaneh, Zhale Hashemi. "A random switching method for PWM cascaded H-bridge multi-level inverter", 2012 IEEE International Conference on Circuits and Systems (ICCAS), 2012
Crossref
16 words — < 1%

19 "Simulation and Prototype Implementation of Hybrid H-bridge MLI with Minimum Switches", International Journal of Engineering and Advanced Technology, 2019
Crossref
15 words — < 1%

20 G. Durga Prasad, V Jegathesan. "FPGA Based Symmetrical Multi Level Inverter with Reduced Gate Driver Circuits", International Journal of Reconfigurable and Embedded Systems (IJRES), 2018
Crossref
15 words — < 1%

21	Shivpal R. Verma, Ankita S Pande, Prashant A. Meshram, Priya P. Gaikwad, Parag G. Shewane, Nitin P. Choudhary. "Implementation of three level H-bridge cascaded multilevel inverter by using AVR microcontroller for SPWM technique", International Journal of Advanced Technology and Engineering Exploration, 2016 Crossref	15 words — < 1%
22	C.D. Townsend, R. Alves Baraciarte, D. Tormo, H. Zelaya De La Parra, G.D. Demetriades, V.G. Agelidis. "Heuristic model predictive modulation in high power multi-level converters", IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, 2015 Crossref	14 words — < 1%
23	trace.tennessee.edu Internet	14 words — < 1%
24	www.aps.com Internet	13 words — < 1%
25	Zi-Yi, Lam, Wong Sew-Kin, Pang Wai-Leong, and Ooi Chee-Pun. "The design of DC motor driver for solar tracking applications", 2012 10th IEEE International Conference on Semiconductor Electronics (ICSE), 2012. Crossref	12 words — < 1%
26	patents.justia.com Internet	12 words — < 1%
27	scienceon.kisti.re.kr Internet	12 words — < 1%
28	vbn.aau.dk Internet	12 words — < 1%

29	Thamizharasan, Sandirasegarane, Seenithangam Jeevananthan, Subburam Ramkumar, Latchumanan Usha Sudha, and Jeevarathinam Baskaran. "Carrierless pulse width modulation strategy for multilevel inverters", IET Power Electronics, 2015. Crossref	11 words — < 1%
30	1library.net Internet	10 words — < 1%
31	Anusha, S., and P V V Rama Rao. "Performance evaluation of sinusoidal PWM technique for a hybrid multilevel power conversion system", 2012 IEEE International Conference on Power Electronics Drives and Energy Systems (PEDES), 2012. Crossref	10 words — < 1%
32	Colak, I.. "Review of multilevel voltage source inverter topologies and control schemes", Energy Conversion and Management, 201102 Crossref	10 words — < 1%
33	www.diodes.com Internet	10 words — < 1%
34	Chulan, Megat Azahari, and Abdul Halim Mohamed Yatim. "Design and implementation of a new H-bridge multilevel inverter for 7-level symmetric with less number of switches", 2014 IEEE International Conference on Power and Energy (PECon), 2014. Crossref	9 words — < 1%
35	K. Muthukumar, T. S. Anandhi, S. P. Natarajan. "81 Levels Trinary Hybrid Cascaded Multilevel Inverter", International Review of Automatic Control (IREACO), 2014 Crossref	9 words — < 1%

36 Madhusudan Singh, Arpit Agarwal, Namrata Kaira. "Performance evaluation of multilevel inverter with advance PWM control techniques", 2012 IEEE 5th India International Conference on Power Electronics (IICPE), 2012 — 9 words — < 1%
Crossref

37 Prakash Singh, Sachin Tiwari, K K Gupta. "A new topology of transistor clamped 5-level H-Bridge multilevel inverter with voltage boosting capacity", 2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 2012 — 9 words — < 1%
Crossref

38 F.-S. Kang, S.-J. Park, M.H. Lee, C.-U. Kim. "An Efficient Multilevel-Synthesis Approach and Its Application to a 27-Level Inverter", IEEE Transactions on Industrial Electronics, 2005 — 8 words — < 1%
Crossref

39 Murugesan Manivel, Lakshmi Kaliappan. "Analysis and Implementation of Switched Capacitor-based Multi-Level Inverter for Electric Vehicles Applications", Elektronika ir Elektrotechnika, 2023 — 8 words — < 1%
Crossref

40 Shivam Prakash Gautam, Manik Jalhotra, Lalit Kumar Sahu, Mano Ranjan Kumar, Krishna Kumar Gupta. "A Survey on Fault Tolerant and Diagnostic Techniques of Multilevel Inverter", IEEE Access, 2023 — 8 words — < 1%
Crossref

41 Vishwajit Kumar, Pooja Kumari, Niranjan Kumar. "Comparison of different levels of cascaded H bridge multilevel inverter using PSPWM technique for EV applications", 2023 IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS), 2023 — 8 words — < 1%
Crossref

42	ent.uthm.edu.my Internet	8 words — < 1%
43	etheses.whiterose.ac.uk Internet	8 words — < 1%
44	hakc.presidioaksforli.it Internet	8 words — < 1%
45	www.researchgate.net Internet	8 words — < 1%
46	www.scribd.com Internet	8 words — < 1%
47	A. Routray, A. Singh, K. Shiluveru, P. Kumar, R. Kumar Singh, R. Mahanty. "REDUCED VOLTAGE STRESS EXTENDABLE SEVENTEEN-LEVEL MULTILEVEL INVERTER USING SINGLE VOLTAGE SOURCE", The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020), 2021 Crossref	7 words — < 1%
48	Advances in Intelligent Systems and Computing, 2016. Crossref	7 words — < 1%
49	Ashish P. Patel, V.J. Rupapara, A. R. Gauswami. "Design and Simulation of 9-Level Hybrid Cascaded H-Bridge Multilevel Inverter with Reduced Components", 2018 International Conference on Current Trends towards Converging Technologies (ICCTCT), 2018 Crossref	7 words — < 1%
50	Dong-Seok Hyun. "A carrierwave-based SVPWM using phase-voltage redundancies for multilevel H-bridge inverter", IECON 99 Conference Proceedings 25th	7 words — < 1%

Annual Conference of the IEEE Industrial Electronics Society (Cat No 99CH37029) IECON-99, 1999
Crossref

51 Ahmad Faiz Minai, Akhlaque Ahmad Khan, Rupendra Kumar Pachauri, Hasmat Malik et al. "Performance Evaluation of Solar PV-Based Z-Source Cascaded Multilevel Inverter with Optimized Switching Scheme", Electronics, 2022 — 6 words — < 1%
Crossref

52 Hema Latha Javvaji, B. Basa Varaja. "Simulation & analysis of different parameters of various levels of cascaded H bridge multilevel inverter", 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), 2013 — 6 words — < 1%
Crossref

53 Saikat Majumdar, Kartick Chandra Jana, Pradipta Kumar Pal, Ariya Sangwongwanich, Frede Blaabjerg. "Design and Implementation of a Single-Source 17-Level Inverter for a Single-Phase Transformer-Less Grid-Connected Photovoltaic Systems", IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022 — 6 words — < 1%
Crossref

EXCLUDE QUOTES	ON	EXCLUDE SOURCES	OFF
EXCLUDE BIBLIOGRAPHY	ON	EXCLUDE MATCHES	OFF