



**SELECTION OF AN INTERMEDIATE REPRESENTATION
FOR PROGRAM ANALYSIS AND OPTIMIZATION**

by

Amar Man Maharjan

A dissertation submitted to the
Central Department of Computer Science and Information Technology,
Tribhuvan University
in partial fulfillment of the requirements for the degree of

**Master of Science in Computer Science and
Information Technology**

TRIBHUVAN UNIVERSITY
Kirtipur, Kathmandu
Nepal

December 2007

Acknowledgements

I am truly thankful to my supervisor and respected teacher Prof. Dr. Shasidhar Ram Joshi, Department of Electronics and Computer Engineering, Institute of Engineering, Pulchowk, for his immeasurable guidance and support to this thesis. I also thank to the Head of the Central Department of Computer Science and Information Technology (CDCSIT) Dr. Tanka Nath Dhamala. Special thanks to my co-supervisor Mr. Samujjwal Bhandari for his kind cooperation, insightful ideas, advice and suggestions.

Many friends and colleagues have contributed greatly to this thesis. Mr. Jagdish Bhatta is the special one who helped me in great deal. Much gratitude to my friends Mr. Bardan S.J.B. Rana, and Mr. Shishir Paudyal also for their incomparable support.

I thank my teachers Prof. Dr. Devi Dutta Paudyal, Prof. Dr. Onkar P. Sharma (Marist College, USA), Asst. Prof. Dr. Subarna Shakya, Asst. Prof. Sudharshan Karanjit, Asst. Prof. Arun Timalina, Mr. Bishnu Gautam, Mr. Hemanta Bahadur G.C. for their invaluable knowledge, support and confidence during my master degree.

CDCSIT's laboratory and its members have provided an excellent environment. In particular, my appreciation goes to Mr. Niraj Manandhar for his technical support. I also thank to all the people who helped me in this thesis directly or indirectly.

And finally, I thank my loving parents and family for their tireless support and patience throughout my life and studies.

Amar Man Maharjan

2007/12/4

Abstract

An Intermediate Representation (IR) is an important part of a compiler. Selecting the right IR can significantly improve not only analyses and optimizations processes of a compiler but also reduce overall time of compiler design. There are many IRs found today but selecting the right IR for compiler is difficult job because different IRs have different properties. In this dissertation, two important IRs, Static Single Assignment (SSA) and Program Dependence Graph (PDG), are studied and presented comparative analyses between PDG and three flavors of SSA form: minimal, pruned and semi-pruned. Selected IRs are implemented in the Machine SUIF compiler infrastructure. PDG pass is implemented in this work but has used Machine SUIF Static Single Assignment Library of Machine SUIF for SSA form. Selected IRs are tested and analyzed with benchmark programs. The results showed that the comparative study presented in this work is very useful to the compiler designer for selecting appropriate IR.

TABLE OF CONTENTS

CHAPTER	PAGE
1. INTRODUCTION	1
1.1 Motivation.....	1
1.2 Compiler.....	2
1.3 Translation Process.....	3
1.3.1 Analysis Phase.....	4
1.3.2 Synthesis Phase.....	5
1.4 Intermediate Representation (IR).....	5
1.5 Comparative Analysis.....	6
1.6 Outline of the Thesis.....	6
2. BACKGROUND	7
2.1 Literature Review.....	7
2.1.1 Sequential IR.....	7
2.1.2 Tree-based IR.....	8
2.1.3 Graph-based IR.....	8
2.2 Tools.....	13
2.2.1 Stanford University Intermediate Format (SUIF).....	13
2.2.2 Machine SUIF.....	13
2.2.3 LCC.....	14
2.2.4 Visualization for Compiler Graphs (VCG).....	14
3. TOOLS AND INTERMEDIATE REPRESENTATIONS' ANALYSIS	15
3.1 Stanford University Intermediate Format (SUIF).....	15
3.1.1 Key features of SUIF System.....	16
3.1.2 The SUIF Architecture.....	16
3.2 Machine SUIF.....	18

3.2.1 Goals of Machine SUIF.....	18
3.3 Static Single Assignment (SSA).....	20
3.3.1 Definition of SSA.....	20
3.3.2 Dominance.....	22
3.3.3 Dominator Trees.....	23
3.3.4 Dominance Frontiers.....	23
3.3.5 Relations between Dominance Frontiers and Joins.....	24
3.3.6 Minimal SSA form.....	25
3.3.7 Pruned SSA form.....	25
3.3.8 Semi-pruned SSA form.....	26
3.3.9 Destruction of SSA form.....	28
3.4 Program Dependence Graph (PDG).....	29
3.4.1 Control Dependence Graph (CDG).....	30
3.4.2 Data Dependence Graph (DDG).....	33
4. IMPLEMENTATION	35
4.1 Implementing Static Single Assignment (SSA).....	36
4.1.1 Implementing minimal SSA form.....	36
4.1.2 Implementing pruned SSA form.....	41
4.1.3 Implementing semi-pruned SSA form.....	41
4.2 Implementing Program Dependence Graph (PDG).....	43
4.2.1 Control Dependence Graph (CDG).....	43
4.2.2 Data Dependence Graph (DDG).....	44
4.3 Inputs and Outputs.....	44
5. TESTING AND ANALYSIS	47
5.1 Empirical Comparison.....	47
5.2 Analysis.....	49
6. CONCLUSIONS	53
6.1 Summary.....	53

6.2 Future Work.....54

REFERENCES **55**

List of Figures

Figure	Page
Figure 1.1 A Compiler.....	2
Figure 1.2 Phases of a Compiler.....	3
Figure 1.3 Position of IR in Compiler.....	6
Figure 2.1 Abstract Syntax Tree.....	8
Figure 2.2 Directed Acyclic Graph.....	9
Figure 2.3 Control Flow Graph.....	9
Figure 2.4 Data Dependence Graph.....	10
Figure 3.1 The SUIF system architecture.....	17
Figure 3.2 Role of SSA form in compilers.....	20
Figure 3.3 (a) a simple control flow graph.....	21
Figure 3.3 (b) its SSA form.....	21
Figure 3.4 Algorithm for building minimal SSA form.....	25
Figure 3.5 Three flavors of SSA form.....	27
Figure 3.6 (a) SSA form.....	29
Figure 3.6 (b) after insertion of copy operation.....	29
Figure 3.7 Structure of PDG.....	30
Figure 3.8 Example of control and data dependencies.....	30
Figure 3.9 (a) Augmented control flow graph.....	32
Figure 3.9 (b) its post-dominator tree.....	32
Figure 3.10 (a) basic control dependence graph	33
Figure 3.10 (b) CDG with region nodes.....	33
Figure 3.11 Example of data dependences.....	34
Figure 4.1 Implementation Structure.....	35
Figure 4.2 Algorithm for building minimal SSA form.....	38
Figure 4.3 Algorithm for calculating DF(X) for each CFG node X.....	39
Figure 4.4 Algorithm for placing ϕ -node.....	40
Figure 4.5 Algorithm for finding non-local names.....	42

Figure 4.6 Algorithm for computing the set $CD(X)$ nodes that are control dependent on.....	43
Figure 4.7 Sample input C program sample.c.....	45
Figure 4.8 Visualization of SSA form in X11.....	46
Figure 4.9 Visualization of PDG in X11.....	46
Figure 5.1 Comparison of construction time between PDG and three flavors of SSA form.....	49
Figure 5.2 Comparison of number of edges between PDG and three flavors of SSA form.....	50
Figure 5.3 Comparison of number of ϕ -nodes between three flavors of SSA form.....	51

List of Table

Table	Page
Table 5.1 Comparing construction time, edges between PDG and SSA, and number of ϕ -nodes between three flavors of SSA form.....	48

List of Abbreviations

IR	Intermediate Representation
SSA	Static Single Assignment
PDG	Program Dependence Graph
SUIF	Stanford University Intermediate Format
MIR	Middle Level Intermediate Representation
AST	Abstract Syntax Tree
DAG	Directed Acyclic Graph
CFG	Control Flow Graph
DDG	Data Dependence Graph
SSI	Static Single Information
VDG	Value Dependence Graph
DFG	Dependence Flow Graph
PDW	Program Dependence Web
VCG	Visualization for Compiler Graphs
OPI	Optimization Programming Interface
NCI	National Compiler Infrastructure
FORTTRAN	Formula Translation
SuifEnv	SUIF Environment