Tribhuvan University
Institute of Science and Technology

Dissertation

"Modification and Evaluation of CFLRU Page Replacement Algorithm for Flash Memory Based System"

Submitted To:

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Student's Declaration

This is to certify that the work is entirely my own and not of any other person, unless explicitly acknowledged (including citation of published and unpublished sources).

Panch Dev Bhatta

Date: 25 February 2016

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Supervisor's recommendation

I hereby recommend that the dissertation prepared under my supervision by **Mr. Panch Dev Bhatta** entitled **"Modification and Evaluation of CFLRU Page Replacement Algorithm for Flash Memory Based System"** be accepted as fulfilling in partial requirements for the degree of Master of Science in Computer Science and Information Technology. In my best knowledge, this is an original work in computer science.

Prof. Dr. Shashidhar Ram Joshi
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LETTER OF APPROVAL

We certify that we have read this dissertation work and in our opinion, it is satisfactory on the scope and quality as a dissertation in the partial fulfillment for the requirement of Master of Science in Computer Science and Information Technology.

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Abstract

Flash disks are becoming an important alternative to conventional magnetic disks because of its positive sides, like more energy-efficient, have no mechanical parts and, therefore, hardly any perceptible latency. Classical buffer replacement policies, like LRU, are not optimal for database systems having flash disks for persistence, because they are not well aware of the distinguished characteristics of those storage devices. CFLRU is one of the page replacement algorithm which partially addresses the flash memory properties. But it has limitations that it cannot reduce the write count when write most reference type pattern occur in real problem. This dissertation work addresses this limitation of CFLRU algorithm and designs modified page replacement algorithm based on CFLRU, named DCH-CFLRU, where second chance is given to hot pages both clean and dirty and replaced cold pages when replacement occurs. This strategy balances and preserves hit ratio and reduce write count. Afterward, the newly designed algorithm is compared and evaluated with basic CFLRU. And based on this experiment the analysis and conclusion have been drawn out.

Experiment and evaluation of this work shows that DCH-CFLRU preserve hit ratio and reduces the write count up to 14% in three workloads. In one workload, read most access, CFLRU gives less write count only when there is large cache size, because large cache can accommodate small number of dirty pages. But this is very rare case in real database system.

Keywords: Page Replacement Algorithm, DCH-CFLRU, CFLRU, Flash Memory

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List of Abbreviations

2Q	-	Two Queue
AD-LRU	-	Adaptive Double Least Recently Used
ARC	-	Adaptive Replacement Cache
CAR	-	Clock with Adaptive Replacement
CFLRU	-	Clean First Least Recently Used
CCFLRU	-	Cold Clean First Least Recently Used
CFDC	-	Clean First Dirty Clustered
CLOCK Pro	-	Clock with Pro
CPU	-	Central Processing Unit
DBMS	-	Database Management System
DCH-CFLRU	-	Dirty Hot Clean Hot Second Chance CFLRU
EELRU	-	Early Eviction Least Recently Used
EEPROM	-	Electrically Erasable Programmable Read Only Memory
FC	-	First Clean
FIFO	-	First In First Out
FTL	-	Flash Translation Layer
GHz	-	Gigahertz
HIR	-	High Inter-reference Recency
HIRS	-	High Inter-reference Recency Set
IRR	-	Inter- Reference Recency
KB	-	Kilo Byte
LFU	-	Least Frequently Used
LIR	-	Low Inter-reference Recency
LIRS	-	Low Inter-reference Recency Set
LIRS-WSR	-	Low Inter-reference Recency Set Write Sequence Reordering
LRFU	-	Least Recently Frequently Used
LRU	-	Least Recently Used
LRU-WSR	-	Least Recently Used Write Sequence Reordering
mA	-	mili Ampere