



Tribhuvan University
Institute of Science and Technology

Dissertation

**“Modification and Evaluation of CFLRU Page Replacement Algorithm for
Flash Memory Based System”**

Submitted To:

Central Department of Computer Science and Information Technology,
Tribhuvan University, Kirtipur, Kathmandu, Nepal

*In Partial Fulfillment of the Requirements for the Degree of Master of Science in
Computer Science & Information Technology (M.SC.CSIT)*

Submitted By:

Mr. Panch Dev Bhatta

(2012-2014, Roll. No.: 13/069)

Central Dept. of Computer Science & Information Technology,
Tribhuvan University

Supervisor:

Prof. Dr. Shashidhar Ram Joshi

Dept. of Electronics & Computer Engineering, IOE, Tribhuvan University, Pulchowk, Nepal

Co-Supervisor:

Mr. Arjun Singh Saud

Faculty

*CDCSIT, Tribhuvan University
Kirtipur, Nepal*



Tribhuvan University
Institute of Science and Technology

**Central Department of Computer Science and Information
Technology**

Student's Declaration

This is to certify that the work is entirely my own and not of any other person, unless explicitly acknowledged (including citation of published and unpublished sources).

Panch Dev Bhatta

Date: 25 February 2016



Tribhuvan University
Institute of Science and Technology

**Central Department of Computer Science and Information
Technology**

Supervisor's recommendation

I hereby recommend that the dissertation prepared under my supervision by **Mr. Panch Dev Bhatta** entitled “**Modification and Evaluation of CFLRU Page Replacement Algorithm for Flash Memory Based System**” be accepted as fulfilling in partial requirements for the degree of Master of Science in Computer Science and Information Technology. In my best knowledge, this is an original work in computer science.

Prof. Dr. Shashidhar Ram Joshi

Dept. of Electronics & Computer Engineering, IOE,
Tribhuvan University, Pulchowk, Nepal

Date: 25 February 2016



Tribhuvan University
Institute of Science and Technology

**Central Department of Computer Science and Information
Technology**

LETTER OF APPROVAL

We certify that we have read this dissertation work and in our opinion, it is satisfactory on the scope and quality as a dissertation in the partial fulfillment for the requirement of Master of Science in Computer Science and Information Technology.

Evaluation Committee

Asst. Prof. Nawaraj Paudel
Head of Department
Central Department of Computer Science
& Information Technology
Tribhuvan University
Kirtipur

Prof. Dr. Shashidhar Ram Joshi
Dept. of Electronics & Computer
Engineering, IOE, Pulchowk,
Tribhuvan University, Nepal
(Supervisor)

(External Examiner)

(Internal Examiner)

Date: 25 February 2016

Acknowledgement

First and foremost, I am sincerely thankful to my supervisor **Prof. Dr. Shashidhar Ram Joshi**, Department of Electronics & Computer Engineering, IOE, who have helped me from beginning of my master degree up to this point and I hope it will continue up to my academic life. This thesis would not have been possible without his guidance, support and endless patience. His vast breadth of knowledge inspired me to learn more and be current with respect to technology trends.

I am equally thankful to my co-supervisor **Mr. Arjun Singh Saud**, faculty member of Central Department of Computer Science and Information Technology, CDCSIT, who gives me the direction for my thesis and timely guidance to accomplish this work.

Most importantly I would like to thank all my respected teachers of CDCSIT Asst. Prof. Nawaraj Paudel (HOD), Prof. Dr. Subarna Sakya, Prof. Dr. Arun Timilshina, Mr. Dheeraj Kedar Pandey, Mr. Jagdish Bhatta, Mr. Min Bahadur Khati, Mr. Sarbin Sayami, Mrs. Lalita Sthapit, Mr. Bikash Balami, Mr. Bishnu Gautam and Mr. Tej Bhadur Shahi for providing me such a broad knowledge, continuous support and inspirations.

My special thanks goes to my senior Mr. Dipak Prasad Bhatt for his valuable support and guidance and to my friends Mr. Harisharan Bhatt, Mr. Shiv Shankar Pant, Mr. Rajesh Pandey, Mr. Pukar Shakya, Mr. Yubraj Dahal, Ms. Deni Shahi and all of my MScCSIT friends for their endless help and company during my master's study period. I am also thankful to all the peoples who have helped me directly and indirectly in completion of this work.

I am grateful toward my department (CDCSIT) of Tribhuvan University for providing this opportunity, because it is beneficial for every student to being mature in his/ her field of study. I have completed this work as I can do. All the future recommendations and suggestions are heartily appreciated.

Last but not least, I would like to thank my parents who always support me in every stage of my life, my brother Indra Dev Bhatta, sisters Kanteshwori, and Santeshwori and their family for their help, love and care.

Abstract

Flash disks are becoming an important alternative to conventional magnetic disks because of its positive sides, like more energy-efficient, have no mechanical parts and, therefore, hardly any perceptible latency. Classical buffer replacement policies, like LRU, are not optimal for database systems having flash disks for persistence, because they are not well aware of the distinguished characteristics of those storage devices. CFLRU is one of the page replacement algorithm which partially addresses the flash memory properties. But it has limitations that it cannot reduce the write count when write most reference type pattern occur in real problem. This dissertation work addresses this limitation of CFLRU algorithm and designs modified page replacement algorithm based on CFLRU, named DCH-CFLRU, where second chance is given to hot pages both clean and dirty and replaced cold pages when replacement occurs. This strategy balances and preserves hit ratio and reduce write count. Afterward, the newly designed algorithm is compared and evaluated with basic CFLRU. And based on this experiment the analysis and conclusion have been drawn out.

Experiment and evaluation of this work shows that DCH-CFLRU preserve hit ratio and reduces the write count up to 14% in three workloads. In one workload, read most access, CFLRU gives less write count only when there is large cache size, because large cache can accommodate small number of dirty pages. But this is very rare case in real database system.

Keywords: Page Replacement Algorithm, DCH-CFLRU, CFLRU, Flash Memory

Table of Contents

| | |
|---|----|
| List of Tables | 6 |
| List of Figures | 7 |
| List of Abbreviations | 8 |
| CHAPTER 1 | 10 |
| BACKGROUND AND PROBLEM FORMULATION..... | 10 |
| 1 Background..... | 10 |
| 1.1 Flash Memory | 10 |
| 1.1.1 NAND Vs. NOR Flash | 11 |
| 1.2 Memory Management | 13 |
| 1.3 Paging..... | 13 |
| 1.4 Page Replacement Algorithm..... | 14 |
| 1.5 Replacement Strategy for Flash Memory Based Systems | 15 |
| 1.6 Performance Metrics | 15 |
| 1.7 Program Behavior | 17 |
| 1.7.1 Working set..... | 17 |
| 1.7.2 Locality of Reference | 17 |
| 1.7.3 Typical Memory Reference Pattern..... | 18 |
| 1.8 Problem Formulation..... | 19 |
| 1.8.1 Basic CFLRU Algorithm..... | 19 |
| 1.8.2 Proposed DCH-CFLRU Algorithm..... | 20 |
| 1.9 Objective | 21 |
| 1.10 Motivation..... | 22 |
| 1.11 Organization of the Thesis | 22 |
| CHAPTER 2 | 23 |
| LITERATURE REVIEW AND METHEDOLOGY | 23 |
| 2 Literature Review..... | 23 |
| 2.1 Traditional Buffer Replacement Algorithms..... | 23 |
| 2.1.1 The Optimal Page Replacement Algorithm..... | 23 |
| 2.1.2 FIFO Page Replacement Algorithm | 23 |

| | | |
|---------------------------|--|----|
| 2.1.3 | LRU Page Replacement Algorithm | 24 |
| 2.1.4 | LRU-K Algorithm | 24 |
| 2.1.5 | NRU Page Replacement Algorithm | 24 |
| 2.1.6 | LFU Page Replacement Algorithm | 24 |
| 2.1.7 | LRFU Page Replacement Algorithm..... | 25 |
| 2.1.8 | 2Q Page Replacement Algorithm | 25 |
| 2.1.9 | ARC Algorithm | 26 |
| 2.1.10 | CLOCK Based Page Replacement Algorithm..... | 26 |
| 2.1.11 | LIRS Algorithm..... | 26 |
| 2.2 | Buffer Replacement Algorithms for Flash-Based Systems..... | 27 |
| 2.2.1 | CFLRU (Clean -First LRU)..... | 27 |
| 2.2.2 | Clean First Dirty Clustered (CFDC)..... | 27 |
| 2.2.3 | LRU-WSR replacement algorithm | 27 |
| 2.2.4 | CCF-LRU | 28 |
| 2.2.5 | LIRS-WSR algorithm | 28 |
| 2.2.6 | AD-LRU (Adaptive Double LRU)..... | 28 |
| 2.3 | Research Methodology..... | 29 |
| CHAPTER 3 | | 30 |
| PROGRAM DEVELOPMENT | | 30 |
| 3.1 | Simulation Environment and Tools..... | 30 |
| 3.2 | Basic CFLRU Algorithm | 30 |
| 3.2.1 | Algorithm: | 30 |
| 3.2.2 | Data Structure | 31 |
| 3.2.3 | Flowchart of Basic CFLRU algorithm | 33 |
| 3.2.4 | Tracing of Basic CFLRU Algorithm | 34 |
| 3.3 | DCH- CFLRU Algorithm | 39 |
| 3.3.1 | Algorithm..... | 39 |
| 3.3.2 | Data Structure | 41 |
| 3.4.2 | Flowchart of DCH-CFLRU Algorithm | 42 |
| 3.4.3 | Tracing of DCH-CFLRU Algorithm | 43 |
| CHAPTER 4 | | 48 |

| | |
|---|----|
| TEST RESULTS & ANALYSIS..... | 48 |
| 4.1 Data Collection..... | 48 |
| 4.2 Testing..... | 49 |
| i) Test Result of Workload 1 (Random Access)..... | 50 |
| ii) Test Result of Workload 2 (Read Most Access)..... | 50 |
| iii) Test Result of Workload 3 (Write Most Access)..... | 51 |
| iv) Test Result of Workload 4 (Zipf Trace Access) | 51 |
| 4.3 Analysis..... | 52 |
| 4.3.1 Hit Ratio Analysis | 52 |
| 4.3.2 Write count Analysis (Line Graph) | 55 |
| CHAPTER 5 | 59 |
| CONCLUSION AND FUTURE WORK | 59 |
| Conclusion..... | 59 |
| Recommendation..... | 59 |
| References..... | 60 |
| Bibliography | 62 |

List of Tables

| | |
|--|----|
| <i>Table 1: The characteristic of flash memory.</i> | 11 |
| <i>Table 2: Basic CFLRU Tracing - State at virtual time 1</i> | 34 |
| <i>Table 3: Basic CFLRU Tracing - State at virtual time 2</i> | 35 |
| <i>Table 4: Basic CFLRU Tracing - State at virtual time 3</i> | 35 |
| <i>Table 5: Basic CFLRU Tracing - State at virtual time 4</i> | 35 |
| <i>Table 6: Basic CFLRU Tracing - State at virtual time 5</i> | 36 |
| <i>Table 7: Basic CFLRU Tracing - State at virtual time 6</i> | 36 |
| <i>Table 8: Basic CFLRU Tracing - State at virtual time 7</i> | 37 |
| <i>Table 9: Basic CFLRU Tracing - State at virtual time 8</i> | 37 |
| <i>Table 10: Basic CFLRU Tracing - State at virtual time 9</i> | 38 |
| <i>Table 11: Basic CFLRU Tracing - State at virtual time 10</i> | 38 |
| <i>Table 12: DCH-CFLRU Tracing - State at virtual time 1</i> | 43 |
| <i>Table 13: DCH-CFLRU Tracing - State at virtual time 2</i> | 44 |
| <i>Table 14: DCH-CFLRU Tracing - State at virtual time 3</i> | 44 |
| <i>Table 15: DCH-CFLRU Tracing - State at virtual time 4</i> | 44 |
| <i>Table 16: DCH-CFLRU Tracing - State at virtual time 5</i> | 45 |
| <i>Table 17: DCH-CFLRU Tracing - State at virtual time 6</i> | 45 |
| <i>Table 18: DCH-CFLRU Tracing - State at virtual time 7</i> | 46 |
| <i>Table 19: DCH-CFLRU Tracing - State at virtual time 8</i> | 46 |
| <i>Table 20: DCH-CFLRU Tracing - State at virtual time 9</i> | 47 |
| <i>Table 21: DCH-CFLRU Tracing - State at virtual time 10</i> | 47 |
| <i>Table 22: Detailed properties of Random Access Reference</i> | 48 |
| <i>Table 23: Detailed properties of Read Most Reference</i> | 49 |
| <i>Table 24: Detailed properties of Write Most Access Reference</i> | 49 |
| <i>Table 25: Detailed properties of Zipf Access Reference</i> | 49 |
| <i>Table 26: Test result of Workload 1 (Random Access) for both algorithm.</i> | 50 |
| <i>Table 27: Test result of Workload 2 (Read Most Access) for both algorithm.</i> | 50 |
| <i>Table 28: Test result of Workload 3 (Write Most Access) for both algorithm.</i> | 51 |
| <i>Table 29: Test result of Workload 4 (Zipf Trace Access) for both algorithm.</i> | 51 |

List of Figures

| | |
|--|----|
| <i>Figure 1: NOR and NAND flash memory array organization.....</i> | 12 |
| <i>Figure 2: Example of basic CFLRU algorithm.</i> | 20 |
| <i>Figure 3: Example of DCH-CFLRU algorithm.</i> | 21 |
| <i>Figure 4: Structure of the Linked List.....</i> | 32 |
| <i>Figure 5: Flowchart of Basic CFLRU</i> | 33 |
| <i>Figure 6: Flowchart of DCH-CFLRU Algorithm.....</i> | 42 |
| <i>Figure 7: Hit ratio analysis for workload 1 (Random Access) for both algorithm.</i> | 52 |
| <i>Figure 8: Hit ratio analysis for workload 2 (Read Most Access) for both algorithm.</i> | 53 |
| <i>Figure 9: Hit ratio analysis for workload 3 (Write Most Access) for both algorithm.</i> | 53 |
| <i>Figure 10: Hit ratio analysis for workload 4 (Zipf Trace Access) for both algorithm.</i> | 54 |
| <i>Figure 11: Write count analysis for workload 1 (Random Access) for both algorithm.</i> | 55 |
| <i>Figure 12: Write count analysis for workload 2 (Read Most Access) for both algorithm.</i> | 56 |
| <i>Figure 13: Write count analysis for workload 3 (Write Most Access) for both algorithm.</i> | 56 |
| <i>Figure 14: Write count analysis for workload 4 (Zipf Trace Access) for both algorithm.</i> | 57 |

List of Abbreviations

| | | |
|-----------|---|---|
| 2Q | - | Two Queue |
| AD-LRU | - | Adaptive Double Least Recently Used |
| ARC | - | Adaptive Replacement Cache |
| CAR | - | Clock with Adaptive Replacement |
| CFLRU | - | Clean First Least Recently Used |
| CCFLRU | - | Cold Clean First Least Recently Used |
| CFDC | - | Clean First Dirty Clustered |
| CLOCK Pro | - | Clock with Pro |
| CPU | - | Central Processing Unit |
| DBMS | - | Database Management System |
| DCH-CFLRU | - | Dirty Hot Clean Hot Second Chance CFLRU |
| EELRU | - | Early Eviction Least Recently Used |
| EEPROM | - | Electrically Erasable Programmable Read Only Memory |
| FC | - | First Clean |
| FIFO | - | First In First Out |
| FTL | - | Flash Translation Layer |
| GHz | - | Gigahertz |
| HIR | - | High Inter-reference Recency |
| HIRS | - | High Inter-reference Recency Set |
| IRR | - | Inter- Reference Recency |
| KB | - | Kilo Byte |
| LFU | - | Least Frequently Used |
| LIR | - | Low Inter-reference Recency |
| LIRS | - | Low Inter-reference Recency Set |
| LIRS-WSR | - | Low Inter-reference Recency Set Write Sequence Reordering |
| LRFU | - | Least Recently Frequently Used |
| LRU | - | Least Recently Used |
| LRU-WSR | - | Least Recently Used Write Sequence Reordering |
| mA | - | mili Ampere |